A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications

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***Abstract*—This paper describes a mixed-signal ECG System-on-Chip (SoC) that is capable of implementing configurable functionality with low-power consumption for portable ECG monitoring applications. A low-voltage and high performance analog front-end extracts 3-channel ECG signals and single channel electrode-tissue-impedance (ETI) measurement with high signal quality. This can be used to evaluate the quality of the ECG measurement and to filter motion artifacts. A custom digital signal processor consisting of 4-way SIMD processor provides the configurability and advanced functionality like motion artifact removal and R peak detection. A built-in 12-bit analog-to-digital converter (ADC) is capable of adaptive sampling achieving a compression ratio of up to 7, and loop buffer integration reduces the power consumption for on-chip memory access. The SoC is implemented in 0.18 μm CMOS process and consumes 32 μW from a 1.2 V while heart beat detection application is running, and integrated in a wireless ECG monitoring system with Bluetooth protocol. Thanks to the ECG SoC, the overall system power consumption can be reduced significantly.**

***Index Terms*—Biopotential recording, ECG, motion artifact reduction, R peak detection, System-on-Chip (SoC).**

I. Introduction

With the increasing use of ambulatory monitoring system, not only continuous signal collection and low-power consumption, but also smartness with robust operation under the patients' daily routine is required. The target is emerging to enable configurability for different applications, ranging from simple heart rate calculation towards more complex medical diagnostics under ambulatory conditions, with extreme low power consumption and high accuracy (Fig. 1).

Especially, one of the major problems in ambulatory ECG monitoring system is the presence of motion artifacts, which lead to poor signal quality, and potentially wrong clinical diagnosis. High signal integrity recording quality and robust operation under the presence of signal artifacts will allow a higher level of physical activity for the subjects. In order to address this challenge, local data processing with advanced functionalities is required, such as motion artifact reduction and accurate feature detection. However these additional functionalities lead to increased computation complexity [1]. Previous solutions using a general purpose processor have limited functionality [2], limited programmability [3], or cannot achieve very low power consumption [4]. Though, the processors [5], [6] are implemented to optimize the biomedical signal processing, they include only the digital processor, so need the external sensor module for biopotential signal acquisition [7], [8]. It increases the system power consumption due to the data transmission between the modules, as well as the system form-factor. This drives the integration of the proposed mixed signal system-on-chip (SoC) combining a low-power analog-front-end (AFE) with a fully optimized and configurable digital signal processor back-end (DBE).

The proposed mixed-signal SoC consists of an AFE that supports continuous and simultaneous monitoring of 3-channel ECG monitoring, with electrode-tissue-impedance (ETI) measurement and band-power (BP) extraction for extracting signal fluctuations in the specified frequency band, with sampling rate of 512-sample/sec and 64-sample/sec, respectively. A 12-bit successive approximation (SAR) analog-to-digital converter (ADC) with adaptive sampling scheme is capable of compressing the ECG data by a factor of 7 before digital signal processing, which in turn reduces the processing power of the DSP and the wireless data transmission [1]. The custom DSP back-end, using SIMD processor architecture, hardwired accelerate unit, effective duty cycling, on-chip memory reduction schemes, and clock gating, provides low power operation while performing multichannel ECG processing. Further, due to the high integration level, a small form-factor can be achieved with minimal use of external components enabling to reduce the system complexity.

This paper is organized as follows. In Section II, we describe the target application of ECG monitoring. Section III and IV describe the details of analog front end and digital back end architecture, respectively. The proposed on-chip memory reduction scheme including the adaptive sampling ADC and the loop buffer is introduced in Section V Finally, chip and system implementation results and test results are described in Section VI, followed by conclusion in Section VII.

II. Target Application Analysis

The advanced functionality such as signal filtering, ECG feature extraction, analysis, and motion artifact suppression

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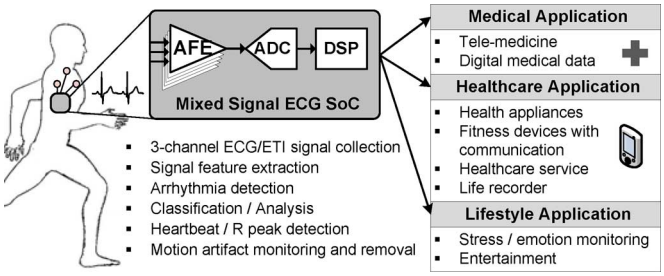

Fig. 1. Mixed-signal ECG SoC and typical applications.

is usually required for the monitoring system. However, the ambulatory systems have very strict requirements in terms of power consumption, signal quality, system complexity, and small form-factor. To meet these requirements, hardware optimization should be achieved on the characteristics of the target application.

A. Motion Artifact Reduction

Ambulatory recording systems suffer from motion artifacts [9], which lead false alarm and wrong event detection. Therefore, the motion artifact needs to be suppressed or cancelled for achieving reliable and high integrity recording quality under ambulatory conditions. Many motion artifact reduction algorithms were introduced, and the traditional algorithms can be classified into two major groups, the adaptive filtering [10]–[12] and the blind source separation method (BSS) [13], [14]. Thanks to the fully integrated ASIC, the ECG SoC can provide both methods according to the necessity.

Adaptive filtering, such as Least Mean Square (LMS) and Recursive Least Squares (RLS), is supposed to act optimally while tracking the non-stationary changes in signal and noise [10], [11]. Adaptive filtering algorithms can be implemented with single channel input. However, in order to achieve high filtering performance, a reference signal having a good correlation with the noise has to be available to estimate the noise characteristics. One or more sensors such as accelerometer have been used for a reference signal. In this work, the electrode-tissue impedance (ETI) signal, which has high correlation with the motion artifact, is introduced for the reference signal [15]. The ETI signal can be recorded continuously and simultaneously together with ECG signal by sharing the electrode, so that the external device is not necessary to be integrated on the system.

Principal Component Analysis (PCA) and Independent Component Analysis (ICA) are widely used algorithms for the BSS method [13], [14], which requires linearly independent multichannel ECG recordings to extract the parameter constructing of eigenvector matrix. The ECG SoC provides simultaneous recording of the three ECG channels, and they are processed with several seconds window to reflect the environment perturbation. BSS method has been well known to achieve the good performance for motion artifacts reduction [13]. However, due to the high algorithm complexity and large window size, they thus require a massive processing power and a large amount of operating memory leading very high power consumption. In this paper, with this limitation, PCA is selected due to its relatively low computational complexity compared to ICA

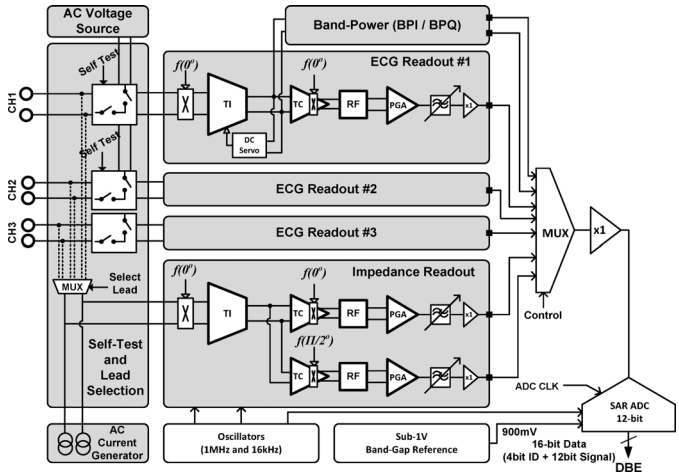

Fig. 2. Block diagram of the analog front end (AFE).

B. Feature Extraction

The feature extraction and the heartbeat classification have been introduced, which are the most essential tools for the analysis of an ECG signal. The feature extraction is investigated by ECG morphology [16], heartbeat interval features [16], [17], derivative-based methods [18], band-power extraction method [1], and frequencybased methods [19]. The accuracy of R peak detection is crucial for reliable analysis, because the R peak contains the primary parameter for arrhythmia analysis like the determination of RR interval and heart-rate-variability (HRV). In this paper, the R peak detection algorithm based on the continuous wavelet transform (CWT) is selected to give the best performance [20]. For the algorithm, wavelet transform with Mexican-hat in the frequency of 15 to 18 Hz is performed repeatedly on the ECG input signal to define the narrow searching window, afterward the R peak is decided by searching the local maximum in the time domain. The CWT-based method achieves the accurate peak detection with a positive predictive value $(+P)$ of 99.8% [20]. Though the CWT-based algorithm provides a high accuracy performance, it is a relatively computationally intensive algorithm due to the repeated convolution operation over all samples. On the other hand, derivative-based methods and band-power methods are used for low power consumption at the expense of a slightly reduced accuracy to predictive value of 99.2% [21].

III. Analog Front End

Fig. 2 shows the architecture of the analog front end (AFE). Each readout channel includes a low-noise and low-power instrumentation amplifier (IA), a ripple filter (RF), a programmable gain amplifier (PGA), and a programmable low-pass filter. The IA is a chopper stabilized current balancing IA [1] redesigned for operation from a 1.2 V supply. The main benefit of this type of IAs is that the common-mode rejection ratio (CMRR) doesn't rely on matching of passives [22], [23] and is able to provide a CMRR in excess of 100 dB. In addition, the AFE also includes a built-in self-test and lead selection block. During the self-test mode, the input leads are connected to a differential on-chip voltage source. This enables the direct measurement of the channel gain and gain matching even

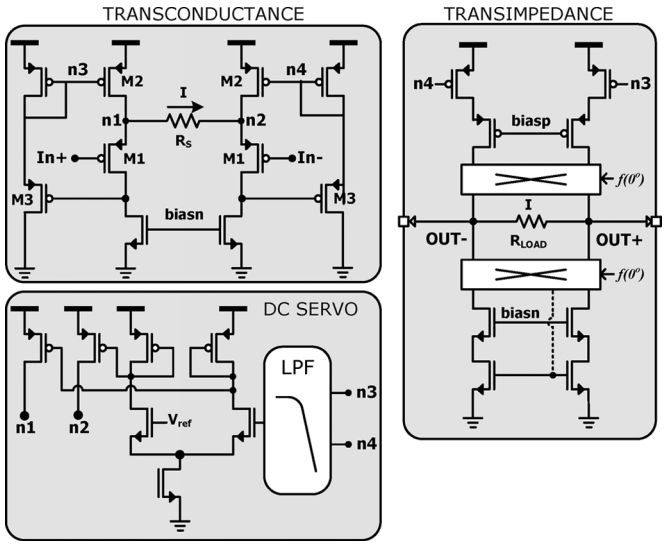

Fig. 3. Architecture of the instrumentation amplifier (IA).

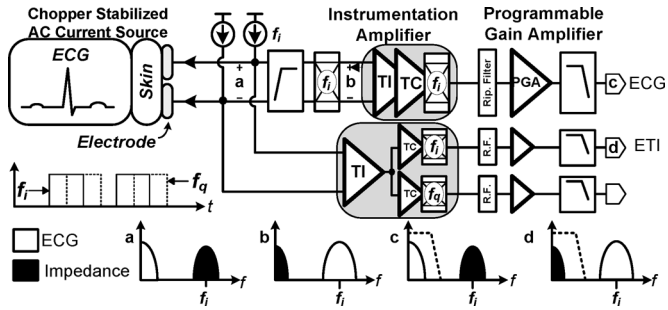

Fig. 4. Continuous electrode tissue impedance (ETI) monitoring circuit.

during remote monitoring applications. On the other hand, the lead selection feature enables the user to monitor the ETI from the selected lead, which in-turn is used in the DSP as a reference signal for the LMS filter for the removal of the motion artifact signals [15]. Two band-power extraction channels (BPI/BPQ) are responsible for extracting the quadrature components of the ECG signal fluctuations in the selected frequency band [1]. In addition to these main functional blocks, all the supporting building blocks have been implemented in the ECG SoC so that the ASIC can be used within a system with a minimal number of external components.

A. Instrumentation Amplifier

The architecture of the IA is shown in Fig. 3. An external floating high pass filter is provided for suppression of differential DC-signals due to electrode polarization [24]. This filter does not suppress common-mode DC signals. So the common-mode input range of the IA is designed to be sufficiently large of 300 mV range. The IA itself is a continuation of the previous generation IA [1], which is a chopper-stabilized current-balancing IA architecture. The complete IA operates within choppers, clocked at 2 kHz to reduce the amplifier 1/f noise [25]. A DC-servo, similar to the one used in [26] is added which operates within the choppers and effectively realizes a high-pass filter for the offset of the transconductance stage (TC) block as well as the chopper-induced offsets.

The IA consists of a transconductance stage (TC) and a transimpedance (TI) output stage. The TC output current can be copied to multiple TI outputs stages, which is useful in the other channels such as ETI and BP extraction channels to reduce the power consumption. The main benefit of the proposed IA architecture is the fact that the input signal sees a gate, which is inherently very high input impedance, and that the amplifier CMRR doesn't depend on matching of passives.

The TC stage is essentially a flipped voltage follower structure [27]. The input transistors M1 act as source followers, as a constant current is forced into them. The differential input voltage appears across the source degeneration resistor $\mathrm{R_s}$. This causes a differential signal current flowing in transistors M2, which is mirrored to the TI output stages. The feedback-loop via transistors M2 implements a $\mathrm{g_m}$-boosting technique, which improves the linearity. Notice that M3 simply implements a DC-shift to prevent M2 to be biased in the linear region. The TC of the circuit is given by

$$G_m = \frac{1}{\frac{1}{g_{m,\mathrm{eff}}} + R_s} = \frac{1}{\frac{g_{01}}{g_{m1}g_{m2}} + R_s}. \tag{1}$$

As long as $\mathrm{R_s}$ is implemented as a linear resistor, the non-linearity is determined by the effective $\mathrm{g_{m,eff}}$. For linear behavior, $\mathrm{g_{m,eff}}$ needs to be large compared to $\mathrm{R_s}$ so that the non-linear term $1/\mathrm{g_{m,eff}}$ is negligible. It is clear from the above formula that as long as $\mathrm{g_{m2}/g_{01}} > 1$, the feedback loop boosts $\mathrm{g_{m1}}$.

As mentioned previously, the DC output is sensed and fed back negatively to the input. Notice that DC here refers to DC within the choppers. The servo will thus eliminate the TC DC-offset and chopper-induced offsets. To this end, the DC voltage is converted to a current which is subtracted from the biasing current at nodes $\mathrm{n_1/n_2}$. The gain is limited to approximately 34 dB in order to linearly amplify differential input signals up to 15 $\mathrm{mV_{pp}}$. The power consumption is 1.7 uA at 1.2 V of which 1.4 uA goes to the TC and the DC-servo and the remaining 300 nA goes to the TI. The total integrated input-referred noise in the frequency band from 0.5 Hz to 100 Hz is measured 1 $\mu\mathrm{V_{rms}}$.

B. Electrical-Tissue Impedance Monitoring

Fig. 4 shows the architecture of the impedance measurement circuit for continuous and simultaneous ETI condition monitoring with the ECG signal. The channel consists of a chopper stabilized IA, a ripple filter and a PGA. Chopper modulation is a power efficient solution for modulating analog signals and shifting their frequency spectrum to a desired frequency with low power consumption [1]. The proposed solution uses chopper modulation to separate the frequency bands of the ETI signal and ECG signal. In addition, the impedance measurement frequency can be made the same as the chopper frequency, which can be as low as twice the ECG signal frequency since the requirement for bandpass filter is eliminated. Lowering the impedance measurement frequency has advantages in terms of evaluating the capacitive part of the electrode impedance, since the impedance of the capacitive part decreases with increasing

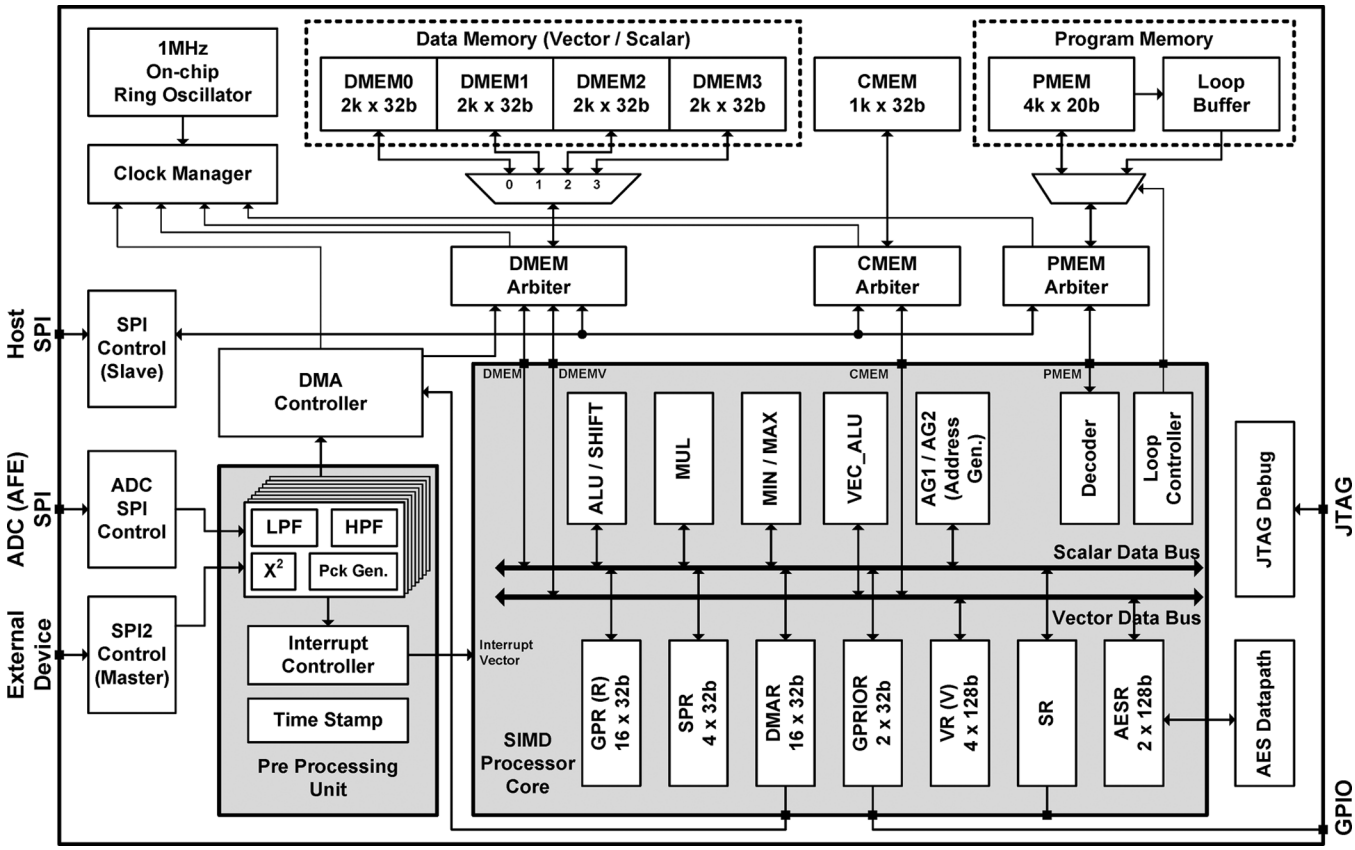

Fig. 5. Block diagram of digital signal processor back-end.

frequency. An important design criterion is to effectively separate the ECG signals and impedance monitoring signals, so that each measurement does not affect the other, minimizing the crosstalk. The possible crosstalk in the ECG channel is related with the order of the low-pass filter, n, and the demodulation frequency, f_i, when the cutoff frequency of the low-pass filter, f_c, is decided. In this design, calculated rejection ratio is less than -18 dB when $n = 2$ and $f_i = 2$ kHz in Fig. 4.

IV. Digital Signal Processing Back-End

Fig. 5 shows the block diagram of the digital signal processor back-end (DBE), which performs user application programs. Like the AFE, the DBE also operates from a 1.2 V supply with a 1 MHz system clock generated by on-chip ring oscillator. The DBE consists of a pre-processing unit, 4-way SIMD, on-chip SRAM for data and program memory, clock management unit, timer, AES-128 accelerator, and several peripheral components. In addition, there are three SPI blocks for accessing the on chip memory, interfacing with ADC interface, and supporting the external device connections, respectively. JTAG and GPIOs are integrated for real-time debugging. 46 kB SRAM is integrated for on-chip data and program memory (PMEM). A data memory (DMEM) consisting of 4 banks can be accessed both by vector and scalar units through the memory arbiter block, and a coefficient memory (CMEM) is integrated to optimize the convolution for parallel data loading. DMA, three SPIs, and processor memory interface are interconnected by a shared bus with priority coding to avoid the memory access congestion. When two or more blocks try to access the memory concurrently, the arbiter gates the clock to halt other contenders.

The pre-processing performs the essential requirement functions before transferring data to the main processor. The primarily tasks for bio signal processing involves the additional bandpass filtering, data packing with sign extension, and stamping the time information for the adaptive sampling scheme. Since the pre-processing should handle ECG input stream in real-time and repeatedly to the every sample, the unit is designed with the dedicated hardware to achieve high throughput.

A direct memory access (DMA) controller supports the sampled data to be written continually into the input buffer in the data memory without interrupting the processor, even when the processor is in sleep mode or running mode with other tasks. 8 DMA channels are prepared for all the input channels from AFE and external device, and each channel can be individually configurable by programming. Once the input buffer is full, an interrupt signal is transferred to the processor for wake-up. 12-system interrupt vectors are prepared for realizing the interrupt service routines (ISR) which are interrupted by DMA transfers, AES-128, and external inputs through the GPIO.

The architecture of fixed-point SIMD processor core is shown in Fig. 6. As mentioned in Section II, a convolution matrix, multiplication, and the trigonometric functions such as sin, cos, and arc-tan for the feature extraction algorithm are computationally very intensive. In order to achieve data-level parallelism and enhance throughput for multichannel processing, the processor core comprises a 128-bit 4-way vector

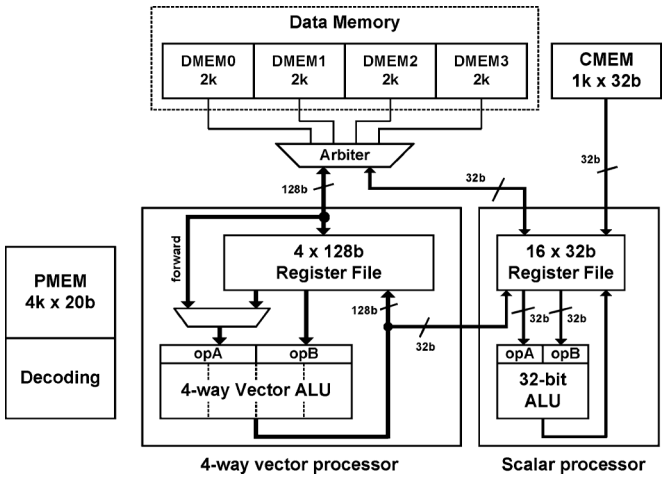

Fig. 6. Parallel architecture of vector unit and scalar unit.

unit, and 32-bit scalar unit with 3-stage pipleline, because the 3 stages pipeline is known as the optimum for low power consumption and transistor utilization [28]. After analysis of the application code, well-defined 20-bit application specific instruction extension and the special datapath are designed to reduce the operating cycles and the program code size.

The 128-bit wide vector unit is responsible for vector and matrix arithmetic operations, which supports the simple logical and arithmetic functions including the special extension instructions. Since multiplication-related instructions spend most of time for the target application, in order to address this issue, the inner dot product (IDP) instruction is implemented in a single cycle, which is given: $Acc = Acc + \sum_{i=0}^{3} A_i \cdot B_i$. The IDP instruction provides parallel execution of vector and scalar unit, which enables parallel data loading from DMEM, 4-way MAD (Multiplication and Add) and a scalar accumulate operations in a single cycle with a single instruction. However, register-register architecture, which both operands are brought from the register files, requires one or two additional cycle for loading the data from the memory into the register. To reduce this latency, the vector unit is designed to support also the register-memory architecture. It enables to bring one operand from the vector register, and the other operand from the data memory directly without a separate load instruction. After fetching the operands, the IDP instruction performs the 32-bit four-way SIMD multiplications and four vector additions including accumulation in a single cycle. For instance, by performing the IDP instruction, throughput of the 16th order FIR filtering can be reduced by 4-cycle, so that it reduces the duty cycle of processing significantly.

AES-128 is applied for the data encryption because it is widely used. Because the AES usually requires the heaviest function with 10 times iteration with 128-bit cipher key and data [29], and the largest portion of the function is contributed on the non-linear operations, it is difficult to execute on general purpose datapath. Therefore, in this work, the dedicated AES-datapath for non-linear operation such as the byte substitution and the mix column is integrated to achieve the high throughput and low power consumption [30]. As a result, AES-128 data encryption rate is achieved to 51-cycle/block.

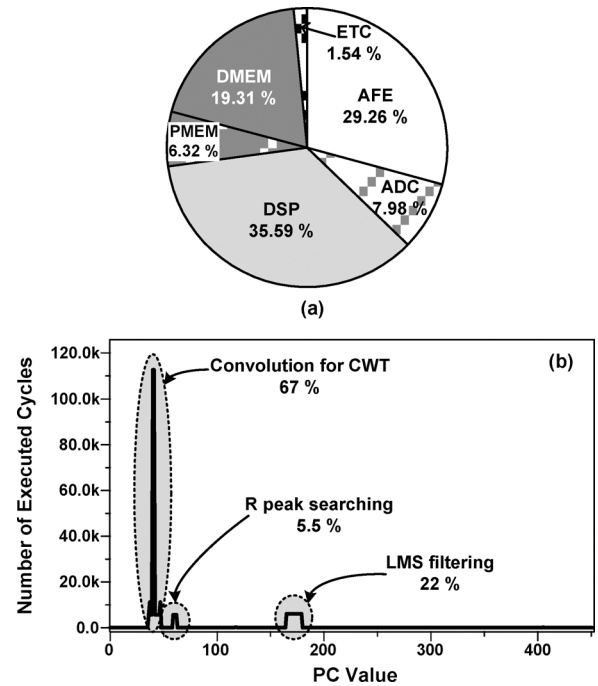

Fig. 7. Analysis of a mixed signal ECG processing platform simulation when CWT-based R peak detection and LMS filtering algorithms are running. (a) Power breakdown of the system. (b) Profiling of the number of execution cycle per program counter (PC). (a) Total power consumption : 71 μW.

In order to achieve low power consumption, the power management is effectively employed. Each channel in AFE has separated power domain, so that only necessary channel can be turned on according to the user application. In digital domain, all 6 clock domains are individually controlled based on the input from the analog domain and issued user program. The digital units are in sleep mode most of the time, and periodically waking up only when the processing unit needs to run. The duty cycle of pre-processing unit and processor core is 2% and 3%, respectively, when running CWT-based R peak detection application.

V. On-Chip Memory Power Reduction

More advanced requirements such as complex medical diagnostics and high accuracy analysis under ambulatory conditions leads to large program code size and large amounts of data that needs to be processed by the DSP and/or transmitted over the radio. A large memory capacity brings not only increase of the area occupation, but also increase of the access and leakage power consumption. Fig. 7(a) shows the power break from the power simulation when R peak detection algorithm is performed with continuous sampling rate of 512 S/s, and the total power consumption is 71-μW. According to the pie chart, we can see that the power consumption for processing and data/program memory accessing are dominated. Therefore, well optimized memory architecture helps reducing the system power significantly. In this work, further on-chip memory power reduction is exploited on both of data memory and program memory.

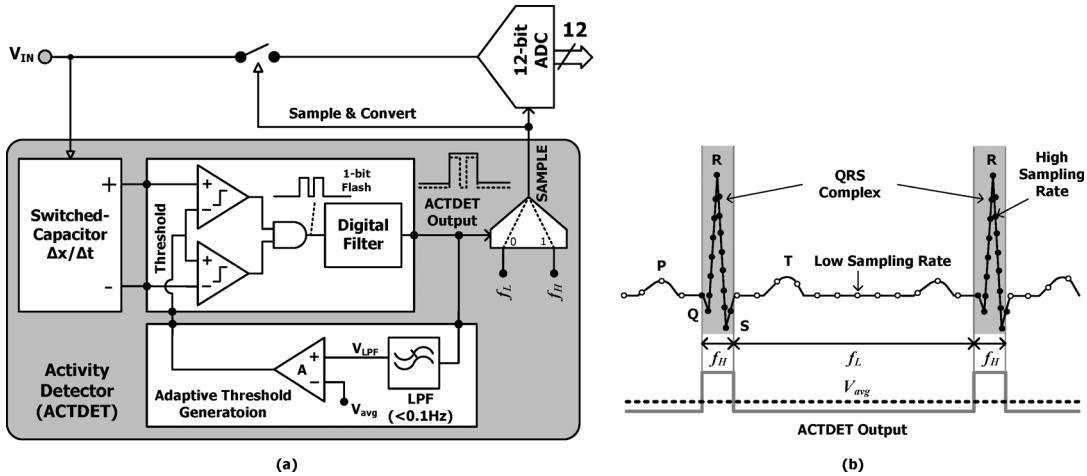

Fig. 8. (a) Architecture of an adaptive sampling ADC. (b) Output of adaptive sampling ADC.

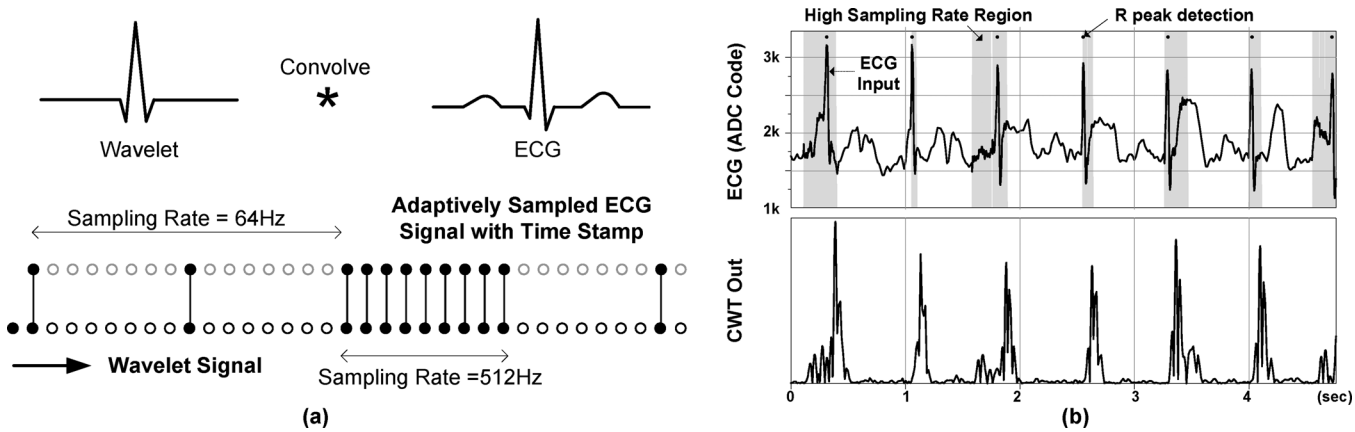

Fig. 9. (a) Applying CWT to an adaptively sampled ECG signals. (b) Measured waveform of R peak detection processing with adaptively sampled ECG signal.

A. Adaptive Sampling ADC for Data Memory Reduction

In general, since the most power consuming part of the monitoring system is the wireless transmission, therefore, more data compression should be achieved prior to the data processing stage to reduce the total system power consumption. Many approaches of ECG signal compression were introduced which are accomplished in both in analog and digital domain [18], [31], [32]. However, the conventional approaches rely on reducing the information content of the signal or still consuming power for the large amount memory accessing, respectively. An alternative approach is to integrate the signal compression in the ADC domain, which is the most attractive in terms of the trade-off between power consumption and reducing the information content of the signal. Furthermore, the data memory optimization can be achieved with data compression in ADC level, by implementing an adaptive sampling ADC [1]. A 12-bit adaptive sampling ADC architecture can adapt its sampling rate between 512 S/s and 64 S/s according to the input signal rate of change.

Fig. 8(a) shows the architecture of the adaptive sampling ADC, which consists of the two major blocks of a 12-bit standard SAR ADC and an activity detector (ACTDET) block. The ACTDET consists of a differentiator, a comparator, and a multiplexer. ACTDET senses the activity of the input signal and selects the sampling rate of the ADC accordingly. In order to do that the input using a switched capacitor differentiator first differentiates signal. The output is digitized by a 1-bit flash ADC, passed through a digital filter, and used to select the sampling rate of the SAR ADC. For simplicity of implementation, only two frequency levels, f_L and f_H, are selected, which are respectively 64 Hz and 512 Hz for this design, as shown in Fig. 8(b). The group delay of ACTDET is 2.5 ms, which can provide detection of the high frequency activity and changing of the ADC sampling rate [1].

The key benefit of such an adaptive sampling scheme is its effect on the average data rate that the system needs to process and transmit over the radio. In order to quantify the benefits of our approach, the CWT-based R peak detection algorithm has been employed on the adaptively sampled input signal and has been integrated into ECG SoC platform. The ECG signal, adaptively sampled by the presented ADC, is fed to the algorithm tailored to process. The only modification has been done to the front-end of the algorithm, i.e., the convolution of the ECG signal with the wavelet. Instead of integrating all the samples, only down sampled date is applied by convolution with the selected wavelet sample as shown in Fig. 9(a). Since the convolution operation

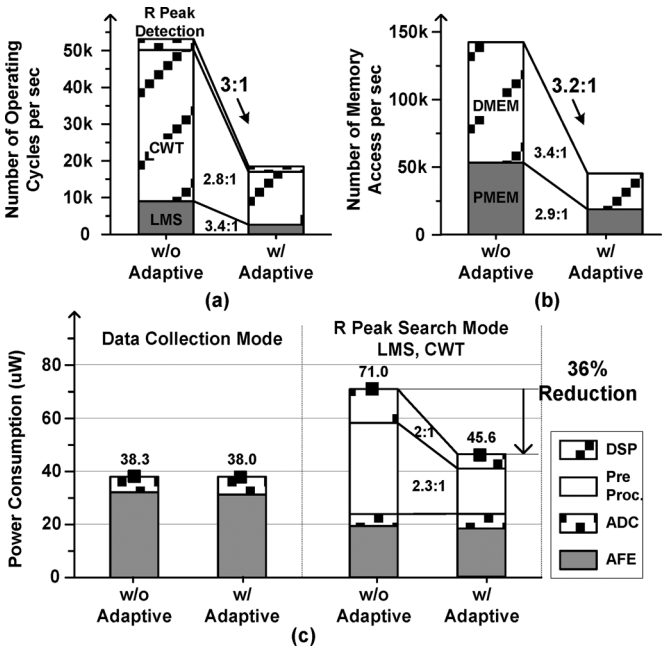

Fig. 10. Performance comparison with adaptive sampling scheme. (a) Number of operating cycle. (b) Number of memory access. (c) Power consumption.

the most time consuming function which has quadratic computational complexity, $O(n^2)$, adaptive sampling significantly reduces the number of multiplications and the memory access during the operation. Fig. 9(b) shows the measured waveforms when the proposed CWT-based R peak algorithm with adaptively sampled signal is applied. We can see that accurate the performance of R peak detection is achieved without any performance degradation. Fig. 10 shows effectiveness of the proposed adaptive sampling scheme on the mixed signal ECG processing platform. The overall operating cycle without adaptive sampling is 53 k cycle/sec. It is reduced by a factor of 3 to 18 k cycle/sec with adaptive sampling. The number of memory access including program and data memory is reduced by 3.2 times as well. The power consumption of the processing using adaptive sampling equivalent to 15% data rate of the full sampling rate corresponds to 50% power reduction in the DSP domain. The overall system power is reduced by 45.6 μW reduced it leads to 36% less overall system power consumption with the adaptive sampling.

B. Loop Buffer for Program Memory Reduction

In bio signal monitoring system, a large amount of execution time is spent in small segments of the application code. As shown in analysis results in Fig. 7(b), 95% of the total execution time is spent in loops of 32 instructions or less, when we run the proposed CWT-based ECG application code. This result is attempting to integrate the loop buffer before the program memory, which supports loop operation with a single instruction fetch.

The processor also supports zero-overhead looping control hardware. Therefore, the loop operation is set using a special instruction, and additional instructions are not needed in order to control the loop. The loop operation is executed a pre-specified number of iteration, which is already known at compile time. The status of this dedicated hardware is stored in the four special registers. Loop Start address register (LS) and Loop End address register (LE) stores the start and the end address of the loop operation, respectively. Loop Count register (LC) keeps the remaining number of iteration, and Loop Flag register (LF) keeps the track of the hardware loop activity. The special instruction for the loops takes the values of LC and LE as input parameters.

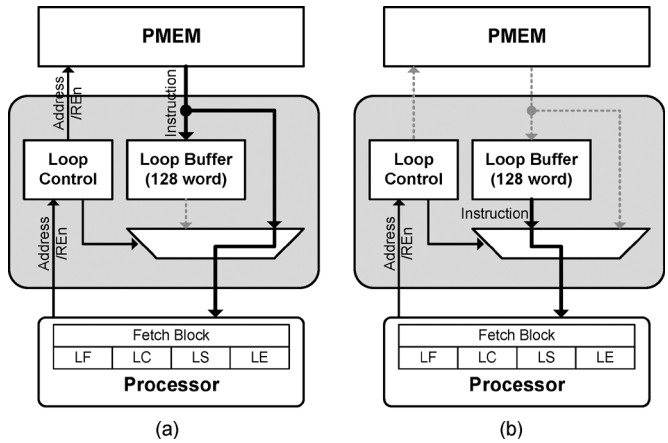

Fig. 11. Program memory organization interface with loop buffer. (a) First iteration of loop. (b) Rest iteration of loop.

Fig. 11 shows the detailed interconnections between the processor core, program memory, and loop buffer. In this work, a 128-word loop buffer is integrated before the program memory. The loop buffer operation is as follows. During the first iteration, the instructions are fetched from the program memory to the loop buffer and the processor [Fig. 11(a)]. The register LF changes its value in the first instruction of the loop body. This change is detected by the state-machine in order to set the proper connections between the different components of the instruction memory organization. The first iteration is taken when the loop buffer records the instructions that the body of the loop contains. Once the loop instructions are kept in the buffer, the instructions are fetched from the loop buffer instead of the program memory during for the rest of the loop iterations [Fig. 11(b)]. At the last iteration, the state-machine detects that the value of the register LC is '1' and sets the connections inside of the instruction memory organization, such that subsequent non-loop instructions are fetched directly from the program memory.

As we can see from the profiling information as shown in Fig. 7(b), the CWT-based ECG application algorithm is a good candidate to perform the energy evaluation, because the execution time of the loops represents approximately 94.5% of the total execution time. As a result, the number of instruction fetches is reduced by 67%, when executing convolution for CWT with a large number of iterations.

VI. Implementation Results and Application

A. Measurement Results

The ECG SoC has been fabricated in a standard 0.18 μm CMOS process and operates from a 1.2 V supply. Fig. 12 shows

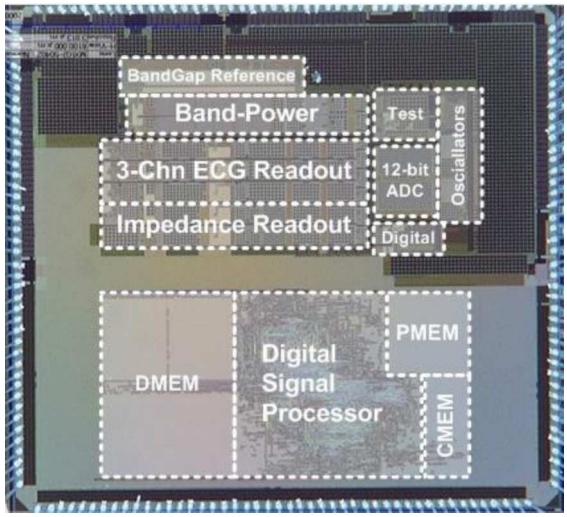

Fig. 12. Die micrograph of the ECG SoC.

TABLE I
PERFORMANCE SUMMARY OF THE ECG SOC

System	Technology	1P6M 0.18μm
	Supply voltage	1.2V
	Area	5mm x 4.7mm (pad limit)
AFE	CMRR	>100dB
	Common-mode input range	200mV – 700mV
	Differential input range	>15mV
	Differential gain (ECG)	75, 150, 200, 300
	Differential gain (ETI)	150, 300, 400, 600
	Bandwidth (ECG & ETI)	150Hz, 200Hz, 250Hz
	RTI noise (.5Hz – 100Hz)	< 1μV_{rms}
ADC	Sampling rate / channel	512 S/s, 64 S/s
	DNL	< 0.4 LSB
	INL	< 4 LSB
DBE	Operating frequency	1MHz
	Memory size (PM, DM, CM)	5kB, 32kB, 4kB
	Data bit-width	32bit

the die micrograph and Table I show the summary of the performance summary. The SoC implements three different real-time monitoring applications:

a) Data collection mode: This mode records the signals continuously and simultaneously from the selected channel. Only AFE, ADC and SPI are running.
b) Beat detection mode: the QRS complex is detected using a derivative-based algorithm [18] or low-power beat detection algorithm with band-power extraction channel [1].
c) Accurate R peak search mode: This mode is necessary for applications with high accuracy. The motion artifact removal algorithm is implemented before the feature extraction stage to enhance the signal reliability and analysis performance. In this paper, two motion artifact removal algorithms are implemented using a low power LMS adaptive filtering and a high-power but higher performance PCA algorithm. Figs. 13 and 14 show the measurement results for both methods.

Fig. 13 shows the measured waveforms when a 4th order LMS filtering is applied. The skin impedance signal, which has a high correlation to the motion artifacts [15], is monitored simultaneously with ECG signal as shown on the top and second plot.

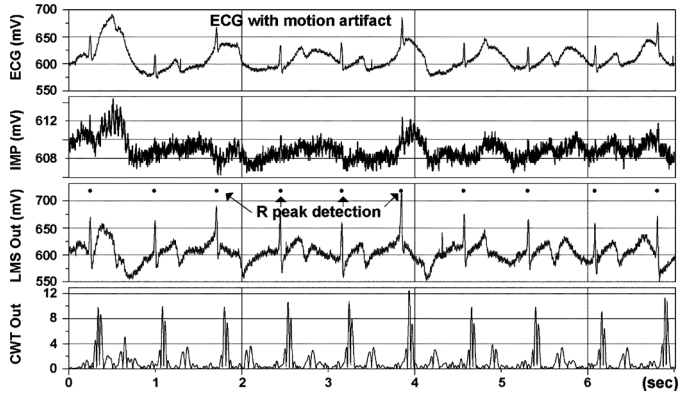

Fig. 13. Measured waveform of motion artifact removal with LMS filter.

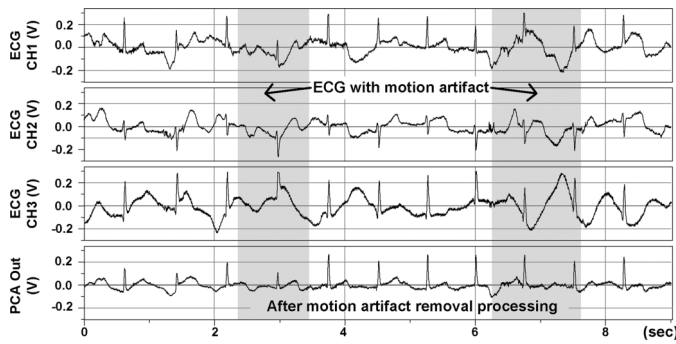

Fig. 14. Measured waveform of motion artifact removal with PCA.

The impedance signal is fed to LMS filter as a noise reference signal. The motion artifact is significantly suppressed with the LMS algorithm as shown in the third plot. Afterwards, a CWT algorithm with Mexican-hat wavelet function [20] is employed to detect the R peak point for more complex medical diagnostics like heart-rate variability (HRV) analysis. The LMS filtering performance is evaluated with the heart beat detection performance, which can be measured by the sensitivity (Se) and the positive predict value $(+P)$. The imec database is used in order to evaluate the filtering performance. The database contains set of the clean ECG signal and the ETI signal for the motion artifact reference signal, and is generated by combining them with specific SNR value, ranging from 10 dB to -10 dB [12]. The input signals were recorded at a sampling rate of 512 Hz during total 10 hours. According to the experimental results, the beat detection performance after applying the proposed algorithm is increased. The beat-detection performance can be achieved a Se and $+P$ of 100% for SNR down to -18 dB and -14 dB, respectively, as compared to Se and $+P$ of unfiltered signal obtaining -16 dB and -9 dB respectively [11]. The ECG SoC consumes 71 μW in this case.

Fig. 14 shows measured waveform of 3-channel ECG monitoring, and its application of the PCA-based motion artifacts reduction algorithm [14]. The electrodes of 3-channels are located over the body with some distance each other in order to achieve the independent signals. The plot shows the independent concurrent 3-channel ECG input signal with noise, and the filtered output. Compared to the LMS filtering, the better motion artifacts reduction performance can be achieved as we can see.

TABLE II
COMPARISON RESULTS WITH STATE-OF-THE-ART

		[5]	[6]	[3]	This Work
Technology		90nm	130nm	180nm	180nm
Performance		1MHz	1 MHz @ 0.7V	64kHz	1MHz @ 1.2V
AFE	**Capability**	No	No	4 ECG/ TIV	3 ECG/ 1 ETI
	ADC			10 bit	12 bit
	power/channel			40uW	17uW
DBE Power	**Beat Detection Mode**	NA	16.4uW	500uW	15.6 uW
	Accurate R Peak Search Mode	47uW	NA		43 uW
Programmability		Yes	Yes	No	Yes
Motion Artifacts Reduction		No	No	No	Yes

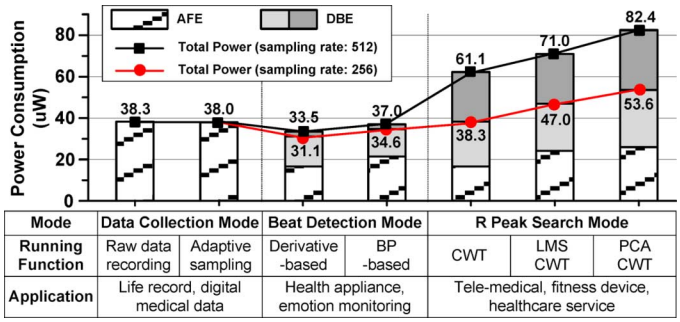

Fig. 15. Power consumption for various user applications.

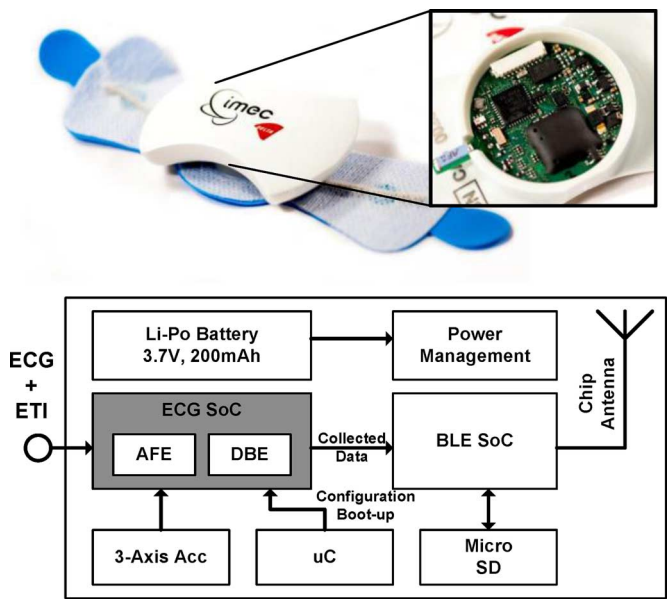

Fig. 16. Photograph and its architecture of the wireless ECG monitoring system utilizing the ECG SoC.

However, due to the algorithm complexity, the power consumption is 82.4 μW, when PCA algorithm with 3-second window size is running.

Fig. 15 shows the overall power consumption for various applications. The complete SoC consumes between 31.1 μW and 82.4 μ W depending on the configuration selected by the user. Table II shows the comparison of system specification with recent ECG monitoring systems with on-chip processing capability. The power number is reported when the ECG monitoring application is running. [5], [6] have lack of an AFE, which enables to increase the total system power consumption with external device integration. While [3] integrates an AFE, however, the digital processing unit is designed with the dedicated hardware, so it can't provide the user application which requires the programmability. Also the overall power consumption is an order of magnitude larger than the other works. The proposed ECG SoC provides high programmability for the various user applications with the lowest power consumption as shown in the Table. Furthermore, by integrating the high performance AFE which provides the concurrent multi-lead monitoring and the ETI signal, the on-chip motion artifacts reduction can be achieved for the robust system operation without the external device integration.

B. ECG Monitoring System Integration

A wireless ECG patch has been developed using the ECG SoC to perform streaming ECG monitoring with real-time motion artifact reduction and arrhythmia detection (Fig. 16). The system consists of ECG SoC, low energy bluethooth SoC (BLE) [33], a 3-axial accelerometer for activity monitoring [34], and a MicroSD card for data logging, and disposable ECG electrodes. The ECG SoC monitors concurrent 3-channel ECG signal and performs the required application, such as motion artifacts reduction and the R peak detection algorithm. The data are processed and analyzed locally, and relevant events and information is wirelessly transmitted in real time and/or stored on a micro SD card. Due to the Bluetooth chip, the system provides connection to PCs and mobile phones through a standard protocol, and maintains very low power consumption for long-term monitoring in home environment.

In order to demonstrate the benefits of the ECG SoC on the system power consumption, three different operation modes have been implemented. The first two modes are streaming data transmission mode. The raw ECG signal and impedance signals are collected at 512 Hz and transmitted without local processing but down sampling with 256 Hz in digital domain. And the second data transmission mode performs a small local processing with only LMS-based motion artifact removal algorithm, and transmit the filtered ECG with 256 Hz sampling rate. On the other hand, in the last mode, the system employs full local processing of accurate R peak search mode with the LMS-based motion artifact removal and CWT-based heart beat detection algorithm using the ECG SoC and transmits only the heart beat rate periodically, once a second (1 Hz). In general, since the most power consuming part is the radio, the last approach, which is as much data processing as possible before

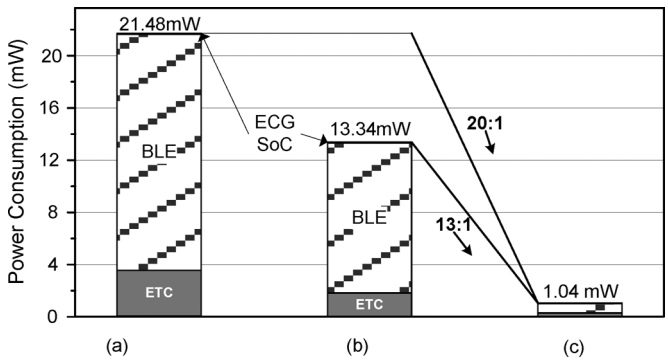

Fig. 17. Power consumption comparison for three different mode.

transmission, is a more efficient method to reduce the total system power consumption. Fig. 17 shows the comparison of the power consumption for the three modes. The overall system power consumption for two streaming mode are 21.48 mW and 1334 mW, respectively, compared to 1.04 mW while providing CWT-based beat detection and transmission of the heart beat rate through the BLE SoC. The ECG SoC still has a negligible impact on the overall power budget, less than 6%, but a significant power reduction by factor of 20 has been achieved. This allows up to one month lifetime with a 400 mAh Li-Po battery and enables the devices for long term monitoring, as well as reduces the size and weight of the system.

VII. Conclusion

This paper presented a mixed-signal ECG SoC, with integrated analog front-end and DSP back-end. The AFE supports concurrent 3-channel ECG monitoring, with impedance measurement and band-power extraction. The custom digital signal processor consisting of a 4-way SIMD processor provides configurability for a wide range of application and advanced functionality like motion artifact removal, accurate R peak detection algorithm, arrhythmia classification and HRV analysis. Various algorithms are possible, allowing different power-performance trade-offs depending on the application requirements. An adaptive sampling ADC significantly reduces the equivalent data-rate of the ADC output without affecting the information content of the input signal, leading to a reduction of data memory access and processing complexity in the DSP domain. The loop buffer integration enables reduction in the access power of the program memory. The presented SoC consumes a best-in-class power consumption of only 31.1 μW from a 1.2 V supply in beat detection mode. The SoC has been integrated in a wireless ECG monitoring system with Bluetooth protocol. Thanks to the advanced features of the SoC like adaptive sampling and local processing, which includes motion artifact removal and accurate R peak detection, the monitoring system can reduce the overall power consumption by factor of 20 compare to a generic system without local processing. This allows to long-term and continuous high integrity signal monitoring and also reduces the system form-factor.

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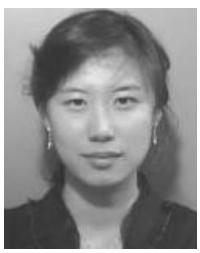

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