# Development of a Bidirectional DC/DC Converter with Dual-Battery Energy Storage for Hybrid Electric Vehicle System

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*Abstract*—**This study develops a newly designed, patented, bidirectional dc/dc converter (BDC) that interfaces a main energy storage (ES1), an auxiliary energy storage (ES2), and dc-bus of different voltage levels, for application in hybrid electric vehicle systems. The proposed converter can operate in a step-up mode (*i.e.*, low-voltage dual-source-powering mode) and a step-down (*i.e.*, high-voltage dc-link energy-regenerating mode), both with bidirectional power flow control. In addition, the model can independently control power flow between any two low-voltage sources (*i.e.*, low-voltage dual-source buck/boost mode). Herein, the circuit configuration, operation, steady-state analysis, and closed-loop control of the proposed BDC are discussed according to its three modes of power transfer. Moreover, the simulation and experimental results for a 1 kW prototype system are provided to validate the proposed converter.**

*Index Terms*—**Bidirectional dc/dc converter (BDC), dual battery storage, hybrid electric vehicle.**

## I. Introduction

Global climate change and energy supply is declining have stimulated changes in vehicular technology. Advanced technologies are currently being researched for application in future vehicles. Among such applications, fuel-cell hybrid electric vehicles (FCV/HEV) are efficient and promising candidates. In the past, Ehsani *et al.* studied the vehicles' dynamics to look for an optimal torque-speed profile of the electric propulsion system [1]. Emadi *et al.* discussed the operating properties of the topologies for different vehicles including HEV, FCV, and more electric vehicles [2]. Emadi *et al.* also integrated power electronics intensive solutions in advanced vehicular power system to satisfy huge vehicular load [3]. Schaltz *et al.* sufficiently divide the load power among the fuel cell stack, the battery, and the ultracapacitors based on two proposed energy-management strategies [4]. Thounthong *et al.* studied the influence of fuel-cell (FC) performance and the advantages of hybridization for control strategies [5]. Chan *et al.* reviewed electric, hybrid, and fuel-cell vehicles and focused on architectures and modeling for energy management [6]. Khaligh and Li presented energy-storage topologies for HEVs and plug-in HEVs (PHEVs). They also discussed and compared battery, UC, and FC technologies. Furthermore, they also addressed various hybrid ESSs that integrate two or more storage devices [7]. Rajashekara reviewed the current status and the requirements of primary electric propulsion components-the battery, the electric motors, and the power electronics system [8]. Lai *et al.* implemented a bidirectional dc/dc converter topology with two-phase and interleaved characteristics. For EV and dc-microgrid systems, the converter has an improved voltage conversion ratio [9]. Furthermore, Lai also studied a bidirectional dc to dc converter (BDC) topology which has a high voltage conversion ratio for EV batteries connected to a dc-microgrid system [10]. In FCV systems, the main battery storage device is commonly used to start the FC and to supply power to the propulsion motor [2, 3]. The battery storage devices improve the inherently slow response time for the FC stack through supplying peak power during accelerating the vehicle [7]. Moreover, it contains a high power-density component such as supercapacitors (SCs) eliminates peak power transients during accelerating and regenerative braking [11]. In general, SCs can store regenerative energy during deceleration and release it during acceleration, thereby supplying additional power. The high power density of SCs prolong the life span of both FC stack and battery storage devices and enhances the overall efficiency of FCV systems [2-8, 12].

A functional diagram for a typical (FCV/HEV) power system is illustrated in Fig. 1 [4, 13]. The low-voltage FC stack is used as the main power source, and SCs directly connected in parallel with FCs. The dc/dc power converter is used to convert the FC stack voltage into a sufficient dc-bus voltage in the driving

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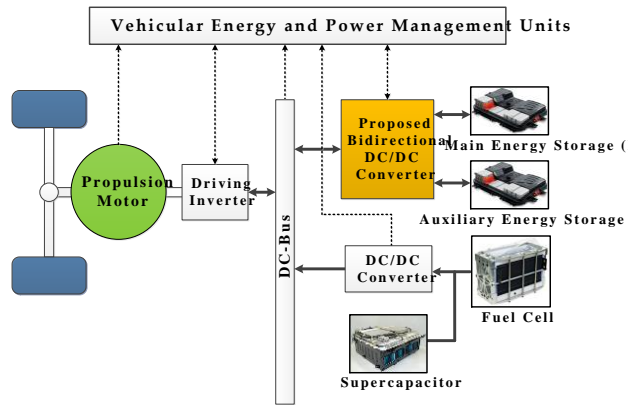
Fig. 1. Typical functional diagram for a FCV/HEV power system.

inverter for supplying power to the propulsion motor. Furthermore, ES1 with rather higher voltage is used as the main battery storage device for supplying peak power, and ES2 with rather lower voltage could be an auxiliary battery storage device to achieve the vehicle range extender concept [13]. The function of the bidirectional dc/dc converter (BDC) is to interface dual-battery energy storage with the dc-bus of the driving inverter.

Generally, the FC stack and battery storage devices have different voltage levels. Several multiport BDCs have been developed to provide specific voltages for loads and control power flow between different sources, thus reducing overall cost, mass, and power consumption [14-27]. These BDCs can be categorized into isolated and nonisolated types.

In isolated converters, high-frequency power transformers are applied to enable galvanic isolation. A few isolated multiport BDC topologies have been investigated, such as the flyback, half- or full-bridge circuits, dual-active bridges, and resonant circuits [14-17, 20, 22, 24]. The literature suggests that nonisolated BDCs are more effective than typical isolated BDCs in EVs [18, 19, 21, 23, 25-27]. Liu *et al.* [18] derived nonisolated multi-input converter topologies by way of a combination of buck, boost, Ćuk, and Sepic. In [23], Wu *et al.* developed the three-port nonisolated multi-input-multi-output (MIMO) converter topologies for interfacing a renewable source, a storage battery, and a load simultaneously. The three double-input converters developed in [19] comprise a single-pole triple-throw switch and only one inductor. A modular nonisolated MIMO converter was presented in [26]. This converter is applied to hybridize clean energy sources of EVs and the basic boost circuit was modified and integrated. However, the voltage gain of the MIMO boost circuit is limited in practice, because of the losses associated with some components such as the main power switch, inductor, filter capacitor, and rectifier diode. To overcome this drawback, three-port power converter that has high-gain characteristic and contains FC, battery sources and stacked output for interfacing HEV, as well as a dc-microgrid was presented [27]. Although the multiport BDC discussed in [25] can interface more than two sources of power and operate at different voltage levels, it

still has limited static voltage gains, resulting in a narrow voltage range and a low voltage difference between the high- and low-side ports.

This study proposes a new BDC topology for FCV/HEV power systems that consists of an interleaved voltage-doubler structure [9, 28] and a synchronous buck-boost circuit. It features two main operating modes: a low-voltage dual-source-powering mode and a high-voltage dc-bus energy-regenerating mode. In addition, the proposed converter can independently control power flow between any two low-voltage sources when in the low-voltage dual-source buck/boost mode. A similar topology was introduced in [29] that only describes a brief concept. By contrast, this study presents a detailed analysis of the operation and closed-loop control of this new topology as well as simulation and experimental results for all its modes of operation. Moreover, this study expanded the topology presented in [29] because the proposed converter can operate over a wider range of voltage levels. The main characteristics of the proposed converter are summarized as follows: 1) interfaces more than two dc sources for different voltage levels, 2) controls power flow between the dc bus and the two low-voltage sources and also independently controls power flow between the two low-voltage sources, 3) enhances static voltage gain and thus reduces switch voltage stress, and 4) possesses a reasonable duty cycle and produces a wide voltage difference between its high- and low-side ports.

The remainder of this paper is structured as follows. The converter topology and operation principle are presented in Section II. The steady state characteristics of the converter, which are based on the operation principle, are analyzed in Section III, whereas Section IV presents the converter control scheme. A 1 kW converter prototype was constructed in this study to validate the proposed converter and demonstrate its merits. The corresponding simulated and experimental results are presented in Section V. Finally, Section VI details the conclusions of this study.

## II. Topology and Operation Modes

The proposed BDC topology with dual-battery energy storage is illustrated in Fig. 2, where $V_H$, $V_{ES1}$, and $V_{ES2}$ represent the high-voltage dc-bus voltage, the main energy storage (ES1), and the auxiliary energy storage (ES2) of the system, respectively. Two bidirectional power switches ($S_{ES1}$ and $S_{ES2}$) in the converter structure, are used to switch on or switch off the current loops of ES1 and ES2, respectively. A charge-pump capacitor ($C_B$) is integrated as a voltage divider with four active switches ($Q_1$, $Q_2$, $Q_3$, $Q_4$) and two phase inductors ($L_1$, $L_2$) to improve the static voltage gain between the two low-voltage dual sources ($V_{ES1}$, $V_{ES2}$) and the high-voltage dc bus ($V_H$) in the proposed converter. Furthermore, the additional $C_B$ reduces the switch voltage stress of active switches and eliminates the need to operate at an extreme duty ratio. Furthermore, the three bidirectional power switches ($S$, $S_{ES1}$, $S_{ES2}$) displayed in Fig. 2 exhibit four-quadrant operation and are adopted to control the power flow between two low-voltage dual sources ($V_{ES1}$, $V_{ES2}$)
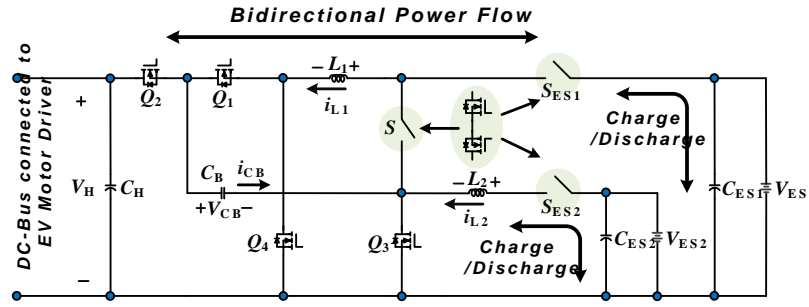
Fig. 2. Proposed BDC topology with dual-battery energy storage.

TABLE I.
CONDUCTION STATUS OF DEVICES FOR DIFFERENT OPERATING MODES

| Operating Modes | ON | OFF | Control Switch | Synchronous Rectifier (SR) |
|---|---|---|---|---|
| Low-voltage dual-source-powering mode (Accelerating, $x_1=1$, $x_2=1$) | $S_{ES1}$, $S_{ES2}$ | $S$ | $Q_3$, $Q_4$ | $Q_1$, $Q_2$ |
| High-voltage dc-bus energy-regenerating mode (Braking, $x_1=1$, $x_2=1$) | $S_{ES1}$, $S_{ES2}$ | $S$ | $Q_1$, $Q_2$ | $Q_3$, $Q_4$ |
| Low-voltage dual-source buck mode (ES1 to ES2, $x_1=0$, $x_2=0$) | $S_{ES1}$, $S_{ES2}$ | $Q_1$, $Q_2$, $Q_4$ | $S$ | $Q_3$ |
| Low-voltage dual-source boost mode (ES2 to ES1, $x_1=0$, $x_2=0$) | $S_{ES1}$, $S_{ES2}$ | $Q_1$, $Q_2$, $Q_4$ | $Q_3$ | $S$ |
| System shutdown | -- | $S_{ES1}$, $S_{ES2}$ $Q_1$, $Q_2$, $Q_3$, $Q_4$ | -- | -- |

and to block either positive or negative voltage. This bidirectional power switch is implemented via two metal-oxide-semiconductor field-effect transistors (MOSFETs), pointing in opposite directions, in series connection.

To explain the concept for the proposed converter, all the conduction statuses of the power devices involved in each operation mode are displayed in Table I. Accordingly, the four operating modes are illustrated as follows to enhance understanding.
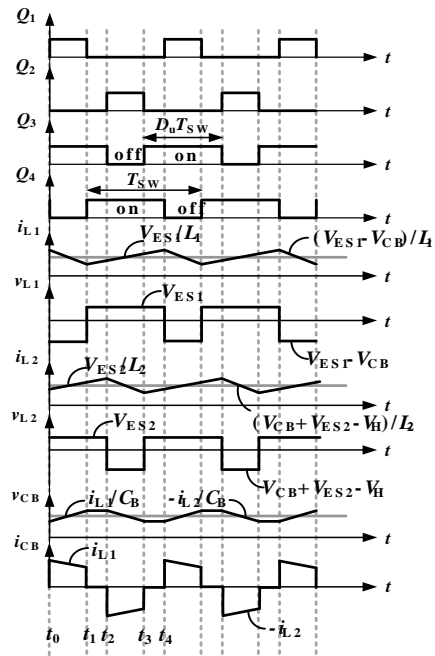
### A. Low-Voltage Dual-Source-Powering Mode

Fig. 3(a) depicts the circuit schematic and steady-state waveforms for the converter under the low-voltage dual-source-powering mode. Therein, the switch $S$ is turned off, and the switches ($S_{ES1}$, $S_{ES2}$) are turned on, and the two low-voltage dual sources ($V_{ES1}$, $V_{ES2}$) are supplying the energy to the dc-bus and loads. In this mode, the low-side switches $Q_3$ and $Q_4$ are actively switching at a phase-shift angle of 180°, and the high-side switches $Q_1$ and $Q_2$ function as the synchronous rectifier (SR).

Based on the typical waveforms shown in Fig. 3(b), when the duty ratio is larger than 50%, four circuit states are possible (Fig. 4). In the light of the on/off status of the active switches and the operating principle of the BDC in low-voltage dual-source-powering mode, the operation can be explained briefly as follows.

**a) State 1 [$t_0 < t < t_1$]:** During this state, the interval time is $(1-D_u)T_{sw}$, switches $Q_1$, $Q_3$ are turned on, and switches $Q_2$, $Q_4$ are turned off. The voltage across $L_1$ is the difference between the low-side voltage $V_{ES1}$ and the charge-pump voltage ($V_{CB}$), and hence $i_{L1}$ decreases linearly from the initial value. In addition, inductor $L_2$ is charged by the energy source $V_{ES2}$,
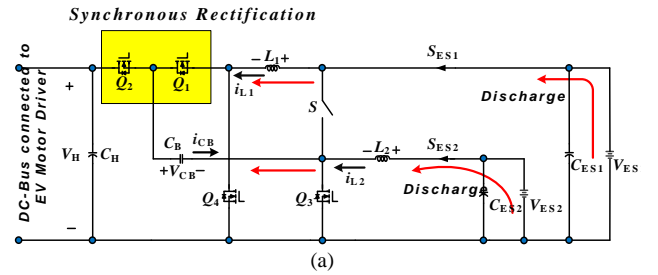


(a)



(b)

Fig. 3. Low-voltage dual-source-powering mode of the proposed BDC: (a) circuit schematic and (b) steady-state waveforms.
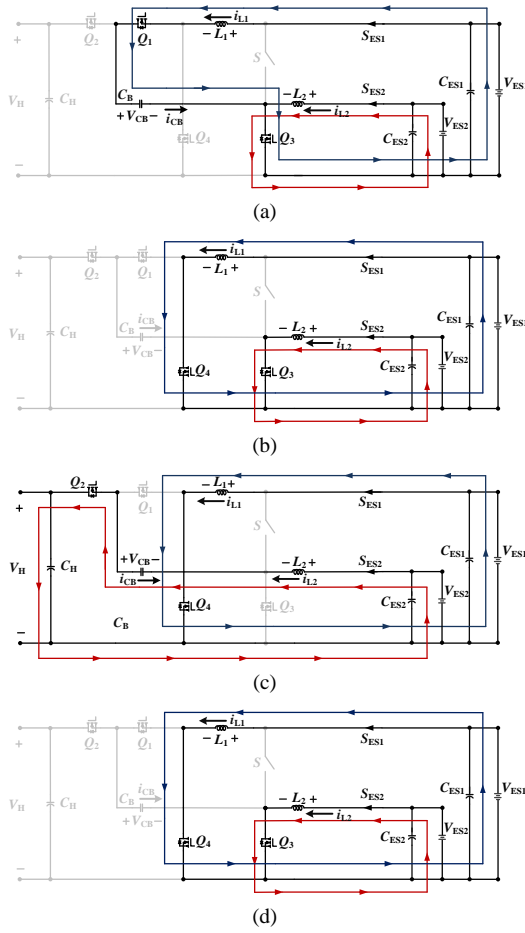
Fig. 4. Circuit states of the proposed BDC for the low-voltage dual-source-powering mode. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

thereby generating a linear increase in the inductor current. The voltages across inductors $L_1$ and $L_2$ can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES2} - V_{CB} \tag{1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2} \tag{2}$$

**b) State 2 [$t_1 < t < t_2$]:** During this state, the interval time is $(D_u-0.5)T_{sw}$; switches $Q_3$ and $Q_4$ are turned on; and switches $Q_1$ and $Q_2$ are turned off. The low-side voltages $V_{ES1}$ and $V_{ES2}$ are located between inductors $L_1$ and $L_2$, respectively, thereby linearly increasing the inductor currents, and initiating energy to storage. The voltages across inductors $L_1$ and $L_2$ under state 2 can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1} \tag{3}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2} \tag{4}$$

**c) State 3 [$t_2 < t < t_3$]:** During this state, the interval time is $(1-D_u)T_{sw}$; switches $Q_1$ and $Q_3$ are turned on, whereas switches $Q_2$ and $Q_4$ are turned off. The voltages across inductors $L_1$ and $L_2$ can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1} \tag{5}$$

$$L_2 \frac{di_{L2}}{dt} = V_{CB} + V_{ES2} - V_H \tag{6}$$

**d) State 4 [$t_3 < t < t_4$]:** During this state, the interval time is $(D_u-0.5)T_{sw}$; switches $Q_3$ and $Q_4$ are turned on, and switches $Q_1$ and $Q_2$ are turned off. The voltages across inductors $L_1$ and $L_2$ can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1} \tag{7}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2} \tag{8}$$

### B. High-Voltage DC-Bus Energy-Regenerating Mode

In this mode, the kinetic energy stored in the motor drive is fed back to the source during regenerative braking operation. The regenerative power can be much higher than what the battery can absorb. Consequently, the excess energy is used to charge the energy storage device. The circuit schematic and the steady-state waveforms of the BDC under the high-voltage dc bus energy-regenerating mode are illustrated in Fig. 5.
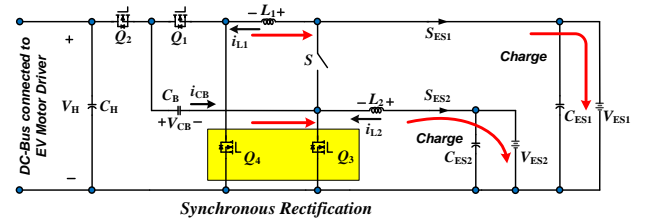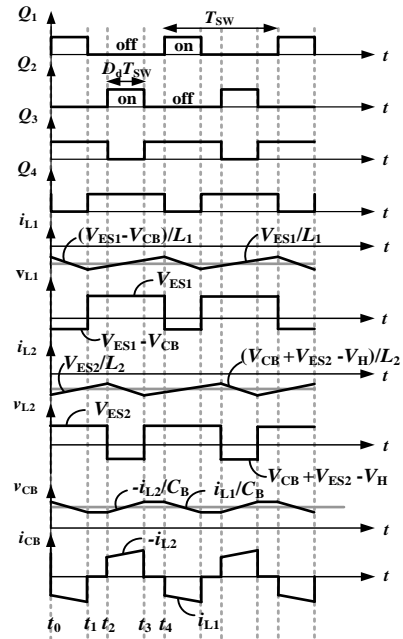


Fig. 5. High-voltage dc-bus energy-regenerating mode of the proposed BDC: (a) circuit schematic and (b) steady-state waveforms.
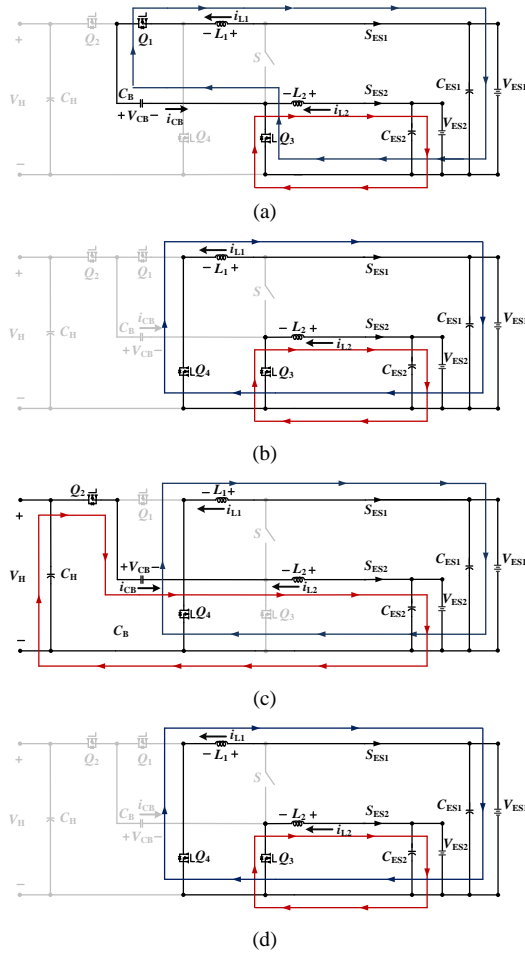
Fig. 6. Circuit states of the proposed BDC for the high-voltage dc-bus energy-regenerating mode. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

Therein, the current in the inductors is controlled by the active switches $Q_1$ and $Q_2$, which have a phase-shift angle of 180° and thereby direct the flow away from the dc-bus and toward the dual energy storage devices; the switches $Q_3$ and $Q_4$ function as the SR to improve the conversion efficiency.

On the basis of the steady-state waveforms shown in Fig. 5(b), when the duty ratio is below 50%, four different circuit states are possible, as shown in Fig. 6. In the light of the on-off status of the active switches and the operating principle of the BDC in high-voltage dc-bus energy-regenerating mode, the operation can be depicted briefly as follows.

**a) State 1 [$t_0 < t < t_1$]:** During this state, the interval time is $D_d T_{sw}$; switches $Q_1$ and $Q_3$ are turned on, and switches $Q_2$ and $Q_4$ are turned off. The voltage across $L_1$ is the difference between the low-side voltage $V_{ES1}$ and the charge-pump voltage $V_{CB}$; hence, the inductor current $i_{L1}$ decreases linearly from the initial value. In addition, inductor $L_2$ is charged by the energy source $V_{ES2}$, which also contributes to the linear increase in the inductor current. The voltages across inductors $L_1$ and $L_2$ can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1} - V_{CB} \tag{9}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2} \tag{10}$$

**b) State 2 [$t_1 < t < t_2$]:** During this state, the interval time is $(0.5 - D_d)T_{sw}$; switches $Q_3$ and $Q_4$ are turned on, and switches $Q_1$ and $Q_2$ are turned off. The voltages across inductors $L_1$ and $L_2$ are the positive the low-side voltages $V_{ES1}$ and $V_{ES2}$, respectively; hence, inductor currents $i_{L1}$ and $i_{L2}$ increase linearly. These voltages can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1} \tag{11}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2} \tag{12}$$

**c) State 3 [$t_2 < t < t_3$]:** During this state, the interval time is $D_d T_{sw}$; switches $Q_1$ and $Q_3$ are turned off, and switches $Q_2$ and $Q_4$ are turned on. The voltage across $L_1$ is the positive low-side voltage $V_{ES1}$ and hence $i_{L1}$ increases linearly from the initial value. Moreover, the voltage across $L_2$ is the difference of the high-side voltage $V_H$, the charge-pump voltage $V_{CB}$, and the low-side voltage $V_{ES2}$, and its level is negative. The voltages across inductors $L_1$ and $L_2$ can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1} \tag{13}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2} + V_{CB} - V_H \tag{14}$$

**d) State 4 [$t_3 < t < t_4$]:** During this state, the interval time is $(0.5 - D_d)T_{sw}$; switches $Q_3$ and $Q_4$ are turned on, and switches $Q_1$ and $Q_2$ are turned off. The voltages across inductors $L_1$ and $L_2$ can be denoted as

$$L_1 \frac{di_{L1}}{dt} = V_{ES1} \tag{15}$$

$$L_2 \frac{di_{L2}}{dt} = V_{ES2} \tag{16}$$

### C. Low-Voltage Dual-Source Buck/Boost Mode

The circuit schematic for this mode, which involves the transfer of energy stored in the main energy storage to the auxiliary energy storage and vice versa is presented in Fig. 7. Therein, the topology is converted into a single-leg bidirectional buck-boost converter.

As shown in Fig. 8, when the duty cycle of the active bidirectional switch $S$ is controlled, the buck converter channels power from main energy storage to the auxiliary energy storage. By contrast, when the duty cycle of switch $Q_3$ is controlled, power flows from the auxiliary energy storage to main energy storage, indicating that the converter is operating in boost mode, as illustrated in Fig. 9.

### III. STEADY-STATE ANALYSIS

In this section, we analyze the voltage gain, switch voltage stress, and uniform average current sharing characteristics of the proposed BDC when operating in a steady state.
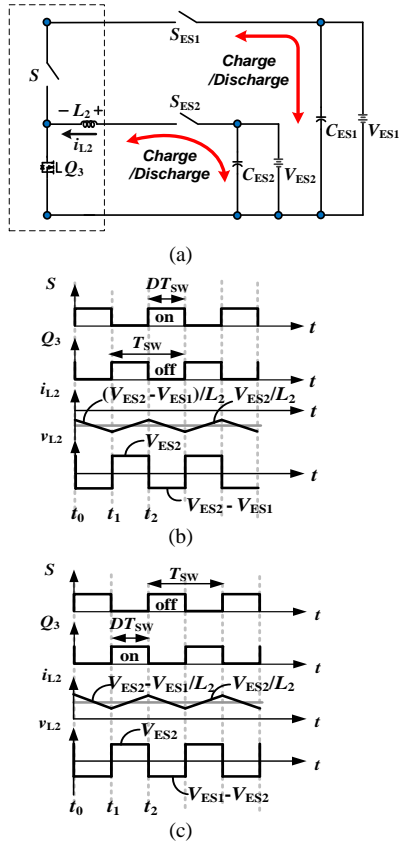
(a)



(b)



(c)

Fig. 7. Low-voltage dual-source buck/boost mode of the proposed BDC: (a) circuit schematic; (b) steady-state waveforms under buck mode; (c) steady-state waveforms under boost mode.
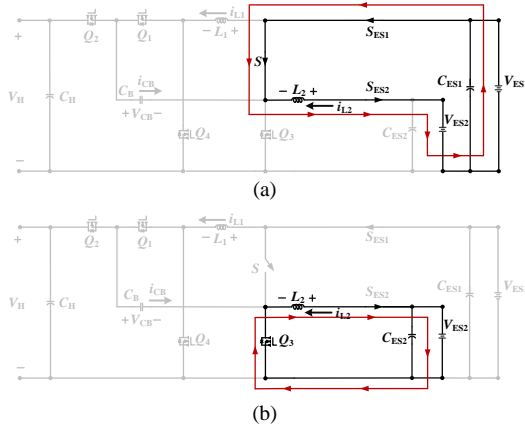


(a)



(b)

Fig. 8. Circuit states of the proposed BDC for the low-voltage dual-source buck mode. (a) State 1. (b) State 2.

*A. Voltage Gain*

The voltage gains of the proposed BDC can be derived by applying the principle of inductor volt-second balance to the different modes. To enhance simplicity and practicality, the equivalent series resistances (ESRs) of the inductors $L_1$ and $L_2$ have been substituted into the state equations as nonideal cases, and the parameters $R_{L1}=R_{L2}=R_L=50\text{m}\Omega$ are also given.
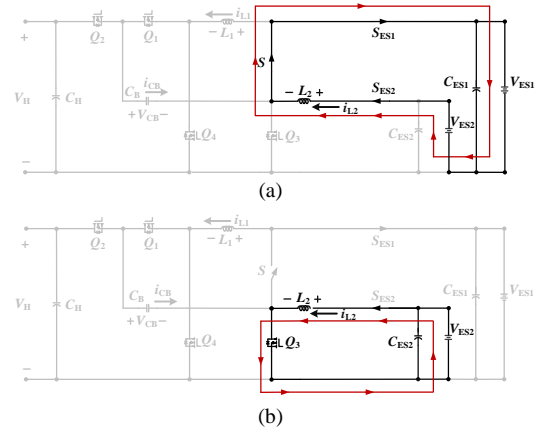


(a)



(b)

Fig. 9. Circuit states of the proposed BDC for the low-voltage dual-source boost mode. (a) State 1. (b) State 2.

*1) Low-Voltage Dual-Source-Powering Mode*

The relationship among the voltage gains of the three dc sources under steady-state operation are given by (17) and (18).

$$\frac{V_H}{V_{s2}} = \left[(k+1) - \frac{2V_{RL}}{V_{s2}}\right]\frac{1}{1-D_u} \tag{17}$$

$$\frac{V_H}{V_{s1}} = \left[\frac{k}{(k+1)} - \frac{2V_{RL}}{V_{s1}}\right]\frac{1}{1-D_u} \tag{18}$$

where $V_{RL}$ is the voltage difference across the ESR of inductance, $k$ is the ratio of $V_{s1}=V_{ES1}$ to $V_{s2}=V_{ES2}$, and $D_u$ is the duty cycle of $Q_3$ and $Q_4$ and is >50%.

Using (17) and (18), the ideal static voltage gains of $V_H/V_{s1}$ and $V_H/V_{s2}$ can be expressed as (19) and (20).

$$\frac{V_H}{V_{s2}} = \frac{k+1}{1-D_u} \tag{19}$$

$$\frac{V_H}{V_{s1}} = \frac{k}{(1-D_u)(k+1)} \tag{20}$$

Accordingly, the relation between dc-bus voltage $V_H$ and the dual-source voltages ($V_{ES1}$, $V_{ES2}$) is given by (21).

$$\frac{V_H}{V_{s1}+V_{s2}} = \frac{1}{1-D_u} \;; V_{s1} = kV_{s2} \tag{21}$$

*2) High-Voltage DC-Bus Energy-Regenerating Mode*

Under steady-state operation, the relationship among the voltage gains of the three dc sources are given by

$$\frac{V_{s1}}{V_H} = (D_d - \frac{2V_{RL}}{V_H})\frac{k}{k+1} \tag{22}$$

$$\frac{V_{s2}}{V_H} = (D_d - \frac{2V_{RL}}{V_H})\frac{1}{k+1} \tag{23}$$

where $D_d$ is the duty cycle of $Q_1$ and $Q_2$ and is <50%.

From (22) and (23), the ideal static voltage gains of $V_{s1}/V_H$ and $V_{s2}/V_H$ are given as (24) and (25).

$$\frac{V_{s1}}{V_H} = \frac{D_d k}{k+1} \tag{24}$$

$$\frac{V_{s2}}{V_H} = \frac{D_d}{k+1} \tag{25}$$

Accordingly, the relation between the dual-source voltages ($V_{ES1}$, $V_{ES2}$) and the dc-bus voltage $V_H$ is given by (26).

$$\frac{V_{s1} + V_{s2}}{V_H} = D_d \;\; ; V_{s1} = kV_{s2} \tag{26}$$

Although these voltage gains are reduced by the ESR of the inductors under the nonideal situation, the parasitic effect is relatively small and thus the reduced voltage gain can be easily compensated for by increasing the duty control.

### 3) Low-Voltage Dual-Source Buck/Boost Mode

The relation between the two low-side voltages is given by (27).

$$\begin{cases} V_{ES2} - V_{RL2} = D_s V_{ES1} \; ; (buck \;\; mode) \\ V_{ES1} = \frac{1}{1-D}(V_{ES2} - V_{RL2}) \; ; (boost \;\; mode) \end{cases} \tag{27}$$

In (27), $D_s$ is the duty cycle of $S$ for the energy transferred from the main energy storage to the auxiliary energy storage, whereas $D$ is the duty cycle of $Q_3$ for the energy transferred from the auxiliary energy storage to the main energy storage. The relationship between the two low-side voltages without the effect of the ESR of inductors can be expressed as (28).

$$\begin{cases} V_{ES2} = D_s V_{ES1} \; ; (buck \;\; mode) \\ V_{ES1} = \frac{V_{ES2}}{1-D} \; ; (boost \;\; mode) \end{cases} \tag{28}$$

### B. Charge-Pump Voltage

The voltage across the $C_B$ under different modes can be derived as follows.

### 1) Low-Voltage Dual-Source-Powering Mode

$$V_{ES1}D_u + (V_{ES1} - V_{CB})(1 - D_u) = 0 \tag{29}$$

$$V_{CB} = \frac{V_{ES1}}{(1 - D_u)} \tag{30}$$

### 2) High-Voltage DC-Bus Energy-Regenerating Mode

$$V_{ES1}(1 - D_d) + (V_{ES1} - V_{ES2})D_d = 0 \tag{31}$$

$$V_{CB} = \frac{V_{ES1}}{D_d} \tag{32}$$

### C. Voltage Stresses on Switches

To simplify the voltage stress analyses of the converter, the voltage ripples on the capacitors were ignored. As shown in Figs. 4, 6, 8, and 9, the maximum voltage stresses of the main power MOSFETs $Q_1 \sim Q_4$ can be obtained directly as (33)-(36).

$$V_{Q_1,\max} = V_H \tag{33}$$

$$V_{Q_2,\max} = V_H - V_{CB} \tag{34}$$

$$V_{Q_3,\max} = V_H - V_{CB} \tag{35}$$

$$V_{Q_4,\max} = 2V_{ES1} - V_{CB} \tag{36}$$

### D. Characteristic of Uniform Average Current Sharing

Through charge balance principles and the state-space averaging technique, the averaged state equations can be obtained directly as

$$\frac{2(i_{L1} - i_{L2})(1 - D_u)}{C_B f_{SW}} = 0 \tag{37}$$

$$\frac{2(i_{L1} - i_{L2})D_d}{C_B f_{SW}} = 0 \tag{38}$$

$$\frac{(i_{L1} + i_{L2})R_H - V_H}{R_H C_H} = 0 \tag{39}$$

where $I_H = V_{CH}/R_H$.

From (37)-(39), the following equation can be obtained:

$$i_{L1} = i_{L2} = \frac{i_H}{2} \tag{40}$$

From (40), the uniform average current sharing can be determined, independent of the values of the capacitors.

## IV. CONVERTER CONTROL

Fig. 10(a) depicts the converter control structure, which consists of a vehicular strategic management level and the proposed BDC controller. The corresponding realized DSP flowchart for selecting operating modes of the proposed BDC is also shown in Fig. 10(b) for reference.

The strategic management level involves an electrical power demand estimation and contains a vehicular power and voltage management unit. The global results of the management must maximize the use of the source that best suits the powertrain power demand, fulfilling the driver and route requirements [21, 25-33]. In FCV/HEV power systems (Fig. 1), the dc-bus voltage of the driving inverter is regulated and powered by the FC stack through a dc-dc converter. Hence, instead of controlling the converter output voltage of each operation mode, the inductor current $i_{L1}$ or $i_{L2}$ is detected and compared with the reference current to control the power flow as shown in Fig. 10(a). In the converter control structure, the vehicular energy and power and voltage management unit selects the BDC mode according to the operating conditions of the vehicle, such as power demand of different driving state ($P_{dem}$) and the dual-source voltages ($V_{ES1}$, $V_{ES2}$). It then selects the appropriate current references $i_{L1,ref}$ or $i_{L2,ref}$ that can control the active switches ($S$, $Q_1 \sim Q_4$) with proportional integral (PI) or more advanced methods. Notably, in spite of it is not easy to choose the optimal parameter of PI controller, the advantages of zero steady-state error and capability of noise filtering, making PI control the most widely used industry algorithm. Furthermore, referring to Table I, two switch selector ($x_1$, $x_2$) of BDC controller can be defined for various operating modes. The pulsed-width-modulation (PWM) switching scheme converts the duty cycle determined by different switch selector statuses into gate control signals for the power switches.
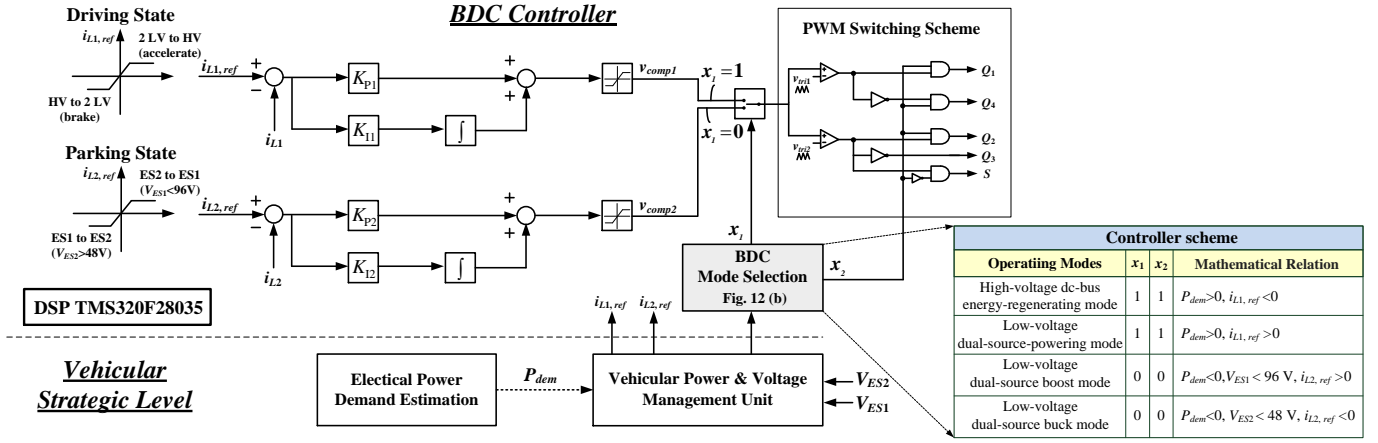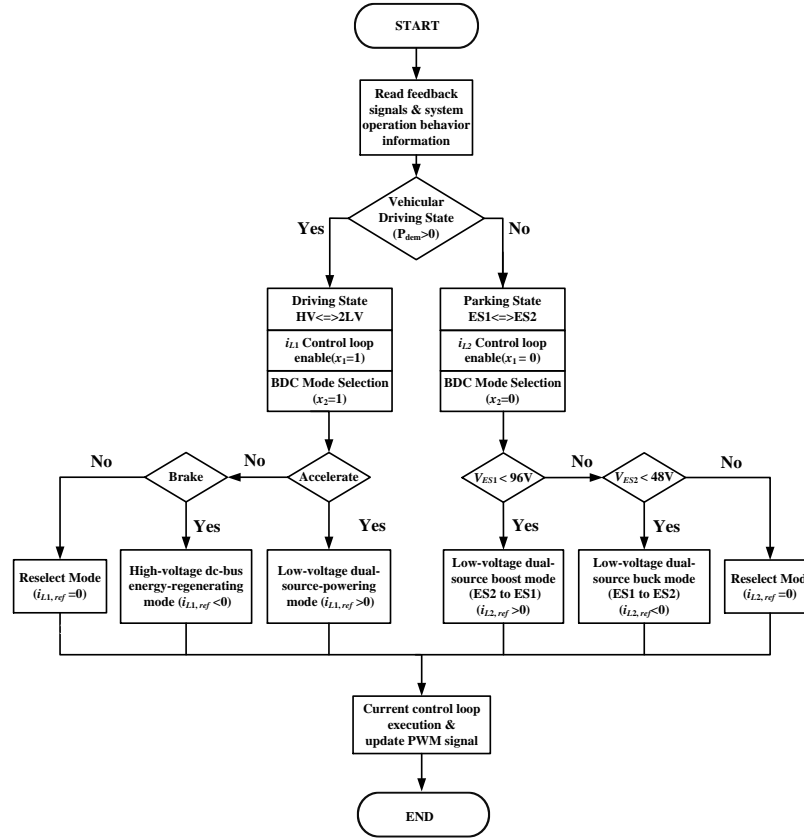
Fig. 10. (a) Block diagram of the closed-loop control scheme; (b) realized DSP flowchart for various operating modes of the proposed BDC.

As Fig. 10(a) displays, the current reference $i_{L1,ref}$ is used to control the bidirectional power flow between the low-voltage dual-source and the high-voltage dc-bus (i.e., 2 LV to HV or HV to 2 LV). In either case, the average inductor current $i_{L2}$ is equal to the controlled average inductor current $i_{L1}$ because of the inherent uniform average current sharing in the proposed BDC topology. By contrast, the current reference $i_{L2,ref}$ is used to control the power flow between the main energy storage and the auxiliary energy storage (i.e., ES1 to ES2 or ES2 to ES1).

The procedure of mode switching is shown in Fig. 10(b) and it is depicted below. First of all, when vehicle is in driving state ($P_{dem}>0$), the controller is $i_{L1}$ control loop ($x_1$=1), and the

controlled switches as shown in Table I (vehicle is accelerating ($i_{L1,ref}>0$, HV to 2 LV) or braking ($i_{L1,ref}<0$, 2 LV to HV)). If neither of the two situations, it will execute reselect mode to process the next judgement of mode switching. Additionally, when vehicle is in parking state ($P_{dem}<0$), the controller is $i_{L2}$ control loop ($x_1$=0), and controlled switches as shown in Table I. In this state, the judgement of mode switching depends on the voltage of $V_{ES1}$ (96 V) and $V_{ES2}$ (48 V). If $V_{ES1}<96$ V, the mode is low-voltage dual-source boost mode ($i_{L2,ref}>0$, $V_{ES2}$ to $V_{ES1}$). When $V_{ES2}<48$ V, the mode is low-voltage dual-source buck mode ($i_{L2,ref}<0$, $V_{ES1}$ to $V_{ES2}$). If both situations do not be satisfied, it executes reselect mode to process the next
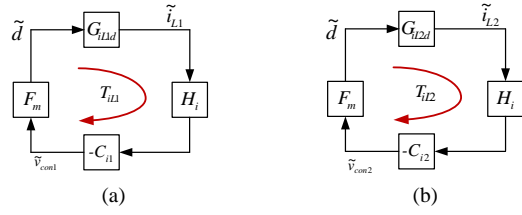
Fig. 11. Block diagram of the closed-loop control scheme for (a) the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes; (b) the low-voltage dual-source buck/boost mode.

judgement of mode switching. Only two closed-loop controllers were developed to control the four power flow conditions based on the average model of the proposed converter derived by using the state-space averaging technique. Fig. 11(a) shows the closed-loop control block diagram that is compatible with both low-voltage dual-source-powering boost mode (i.e., 2 LV to HV) and high-voltage dc-bus energy-regenerating mode (i.e., HV to 2 LV); the closed-loop control block diagram displayed in Fig. 11(b) is compatible with the low-voltage dual-source buck/boost mode (i.e., ES1 to ES2 or ES2 to ES1).

In Fig. 11, $F_M$ represents the constant gain of the PWM generator; $G_{iL1d}$ denotes the transfer function, which converts the duty cycle to inductor current $i_{L1}$; $G_{iL2d}$ is the transfer function from duty cycle to inductor current $i_{L2}$; $C_{i1}$ and $C_{i2}$ represent the transfer function of inductor current controllers, and $H_i$ is the sensing gain of the current sensor.

To design the closed-loop controller and simplify the mathematics of the proposed BDC, the PSIM$^{©}$ circuit model is built under the following three assumptions: 1) power switches and diodes are ideal; 2) equivalent series resistances of all inductors and capacitors of the converter are considered to obtain a relatively precise dynamic model; and 3) the converter is operated under a continuous conduction mode.

In the PSIM$^{©}$ circuit model, the adopted circuit parameters are $L_1=L_2=250$ µH, $C_B=10$ µF, $C_H=1880$ µF, $C_{ES1}=C_{ES2}=400$ µF, the ESR of inductances $R_{L1}=R_{L2}=R_L=50$ mΩ and ESR of capacitances $R_{CB}=20$ mΩ, $R_{ES1}=R_{ES2}=50$ mΩ, and line resistances $R_{ES1}=12$ mΩ and $R_{ES2}=6$ mΩ. Based on these assumptions, the design of the two closed-loop controllers are illustrated in the following sections.

*A. Controller for Low-Voltage Dual-Source-Powering and High-Voltage DC-Bus Energy-Regenerating Modes*

Under these two modes, the open-loop gain of the current loop of the proposed BDC can be derived as

$$T_{iL1} = F_m G_{iL1d} H_i C_{i1} \tag{41}$$
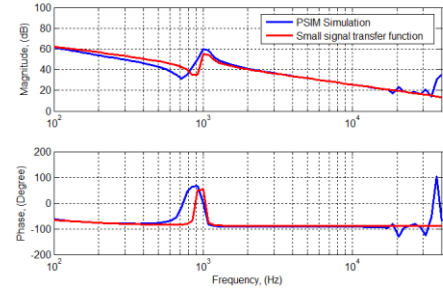
where $F_M=1/100$, $H_i=1$.



Fig. 12. Loop gain frequency responses of uncompensated current loop in the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes.
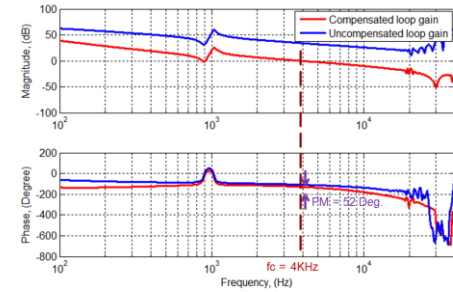


Fig. 13. Loop gain frequency responses of compensated current loop in the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes.

To simply the derivation, we assume that the dc-bus voltage $V_H$ and the dual energy source voltage ($V_{ES1}$, $V_{ES2}$) are constant; beside, the key circuit parameters ($C_B$, $L_1$, $L_2$, $R_{CB}$, $R_{L1}$, $R_{L2}$) are used to derive the small-signal transfer function $G_{iL1d}$ from the duty cycle to the inductor current $i_{L1}$, as (42). Substituting the above-mentioned circuit parameter values into (42), the numerical result can be expressed by third-order transfer functions as shown in (43).

To check the correctness, Fig. 12 shows the fitting curves made by Matlab$^{©}$ and PSIM$^{©}$ simulation software, and the results are closely between each other. Furthermore, in Fig. 12, the observable resonant behavior around 1-kHz is caused by three poles and two zeros that induced from the circuit parameters ($C_B$, $L_1$, $L_2$). The corresponding current controllers of the proposed converter under both low-voltage dual-source-powering and high-voltage dc-bus energy-regenerating modes are selected as

$$C_{i1} = 0.02 \cdot (1 + \frac{2000}{s}) \tag{44}$$

Fig. 13 shows the loop-gain frequency response of the compensated current loop in low-voltage dual-source-powering and high-voltage dc-bus energy-regenerating modes, under full-load conditions; this design results in a phase margin of 52° and a crossover frequency of approximately 4 kHz.

$$G_{iL1d} = \frac{\hat{i}_{L1}}{\hat{d}} = \frac{(L_1 C_B V_{CB})s^2 + (L_1 i_L R_{CB} + R_L C_B V_{CB} + C_B V_{CB} R_{CB} D_u)s + (1-D_u)V_H + (i_L R_{CB})(R_L + R_{CB} D_u)}{C_B L_1 (L_1 R_L + R_{CB} + R_{CB} D_u)s^3 + C_B L_1 [R_L^2 + R_{CB} R_L + R_{CB} D_u (R_{CB} D_u + R_L + 2R_{CB})]s^2 + 2L_1(1-D_u)^2 s + 2(1-D_u)^2(R_L + R_{CB})} \tag{42}$$

$$G_{iL1d} = \frac{(1.53 \times 10^{-6})s^2 + (3.76 \times 10^{-4})s + 48.2}{(1.28 \times 10^{-12})s^3 + (6.36 \times 10^{-10})s^2 + (5.38 \times 10^{-5})s + 0.016} \tag{43}$$
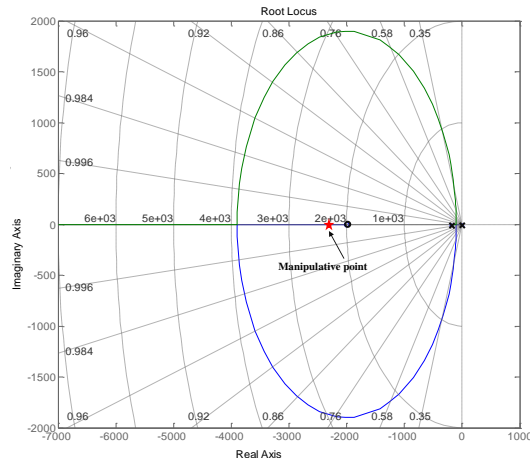
Fig. 14. Root locus of compensated current loop in the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes.
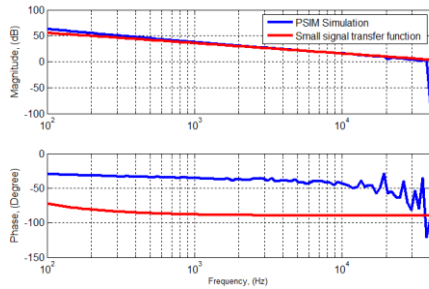


Fig. 15. Loop gain frequency responses of uncompensated current loop in the low-voltage dual-source buck/boost mode.

Fig. 14 shows the root locus of compensated current loop in the low-voltage dual-source-powering and the high-voltage dc-bus energy-regenerating modes. The result of compensation has four poles and three zeros that all on the left side of imaginary axis baseline, by contrast, if there is any pole or zero point on the right side of imaginary axis baseline, the designed controller will be unstable. As a result, the controller is stable and the manipulative point is pinpointed on Fig. 14.

*B. Controller for Low-Voltage Dual-Source Buck/Boost Mode*

In this mode, the open-loop gain of the current loop of the proposed BDC can be derived as

$$T_{iL2} = F_m G_{iL2d} H_i C_{i2} \tag{45}$$

where $F_M = 1/100$, $H_i = 1$.

The small-signal transfer function $G_{iL2d}$ from the duty cycle to the inductor current $i_{L2}$ can be represented as follows.

$$G_{iL2d} = \frac{\hat{i}_{L2}}{\hat{d}} = \frac{V_{ES1}}{sL_2 + R_{L2}} = \frac{96}{2.5 \times 10^{-4} s + 5 \times 10^{-2}} \tag{46}$$

To check the correctness, Fig. 15 shows the fitting curves made by Matlab© and PSIM© simulation software, and the results are closely each other. The corresponding current controllers of the proposed converter in low-voltage dual-source buck/boost mode are selected using (47) below.
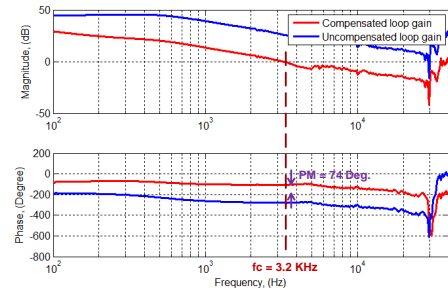


Fig. 16. Loop gain frequency responses of compensated current loop in the low-voltage dual-source buck/boost mode.
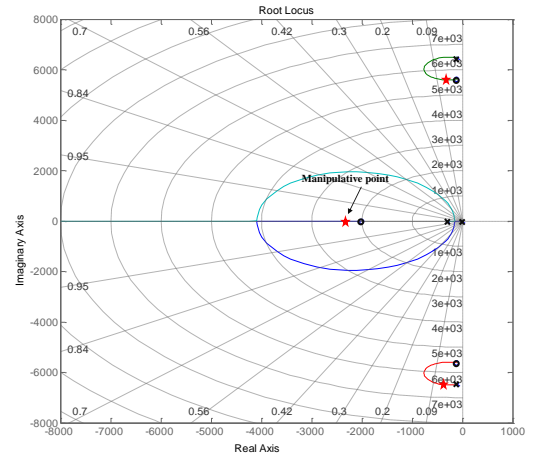


Fig. 17. Root locus of compensated current loop in the low-voltage dual-source buck/boost mode.

$$C_{i2} = 0.05 \cdot (1 + \frac{2000}{s}) \tag{47}$$

Fig. 16 illustrates the loop-gain frequency response of the compensated current loop in low-voltage dual-source buck/boost mode, under full-load conditions; this design results in a phase margin of 74° and a crossover frequency of approximately 3.2 kHz.

Fig. 17 shows the root locus of compensated current loop in the low-voltage dual-source buck/boost mode. The result of compensation has two poles and one zeros that all on the left side of imaginary axis baseline, by contrast, if there is any pole or zero point on the right side of imaginary axis baseline, the designed controller will be unstable. As a result, the controller is stable and the manipulative point is pinpointed on Fig. 17.

V. SIMULATION AND EXPERIMENTAL RESULTS

Simulations and experiments were conducted to verify the performance of the proposed model. A 1 kW laboratory prototype was constructed according to the specifications and parameters presented in Table II. A photograph of the realized BDC prototype and the test bench are shown in Fig. 18. DC voltage sources and electric loads were substituted for the main energy storage and the auxiliary energy storage. The system developed in this study included two loads for the high-voltage dc-bus energy-regenerating mode and two sources for the low-voltage dual-source-powering mode. In this experimental

TABLE II.
SPECIFICATIONS AND PARAMETERS OF THE PROTOTYPE SYSTEM

| Specifications | |
|---|---|
| ES1 voltage | $V_{ES1}$: 96 V |
| ES2 voltage | $V_{ES2}$: 48 V |
| DC-bus voltage | $V_H$: 430 V |
| Output power | $P_o$: 1 kW |
| Switching frequency | $f_{SW}$: 40 kHz |
| **Parameters** | |
| Inductors | $L_1$, $L_2$: CH330060, 250 uH |
| High-side capacitor | $C_H$: aluminum capacitor, 1880 μF |
| Low-side capacitor | $C_{ES1}$: aluminum capacitor, 400 μF<br>$C_{ES2}$: aluminum capacitor, 400 μF |
| Charge-pump capacitor | $C_B$: film capacitor, 10 μF |
| Switches | $S$, $S_{ES1}$, $S_{ES2}$: IXFK360N15T2<br>$Q_1$, $Q_4$, $Q_2$, $Q_3$: W45NM60 |
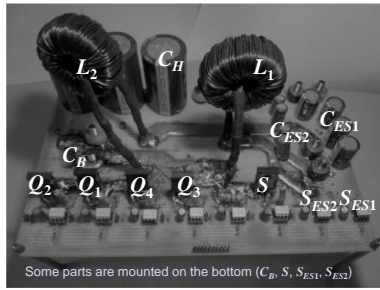


(a)
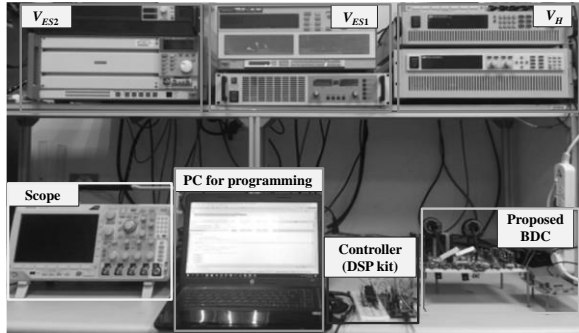


(b)

Fig. 18. Photograph of the realized BDC prototype and the test bench system. (a) BDC prototype; (b) test bench system.

setup, a general purpose Texas Instrument Piccolo DSP kit on a TMS320F28035 fixed-point 32-bit/60MHz CPU was used to generate the PWM control signals.

PSIM© simulation software was also applied to verify the feasibility of the proposed BDC. Fig. 19 illustrates that both sources powered the traction motor, thereby boosting the two input voltages. Therefore, both sources contributed to the dc-bus voltage $V_H$ of 430V.

The observations on the power flow from the dc-bus to the main energy storage and the auxiliary energy storage are detailed in Fig. 20. Inductor currents $i_{L1}$ and $i_{L2}$ flowed in a direction opposite that of the input power. The low-side output voltages $V_{ES1}$ and $V_{ES2}$ were approximately 96V and 48V, respectively.

Fig. 21 illustrates the experimental waveforms for the low-voltage dual-source buck mode and the boost mode. The directions of the inductor currents in Fig. 21(a) are opposite to
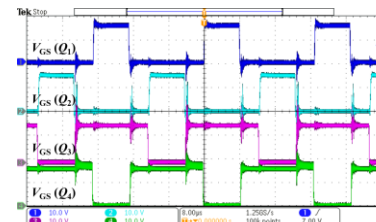


(a)
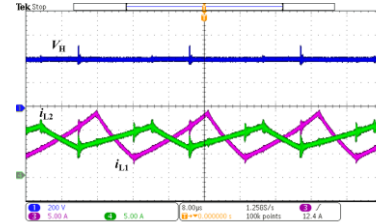


(b)

Fig. 19. Measured waveforms for low-voltage dual-source-powering mode: (a) gate signals; (b) output voltage and inductor currents.
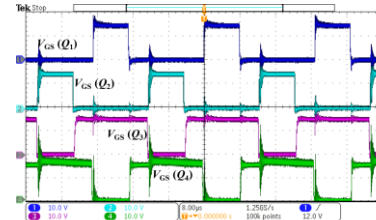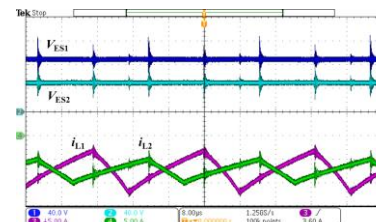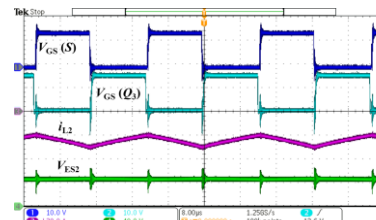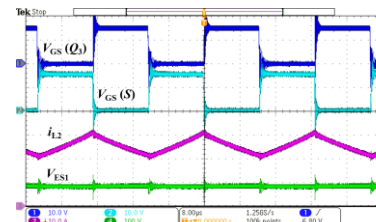


(a)



(b)

Fig. 20. Measured waveforms for high-voltage dc-bus energy-regenerating mode: (a) gate signals; (b) output voltage and inductor currents.



(a)



(b)

Fig. 21. Measured waveforms of gate signals, output voltage and inductor currents for the low-voltage dual-source buck/boost mode: (a) buck mode; (b) boost mode.
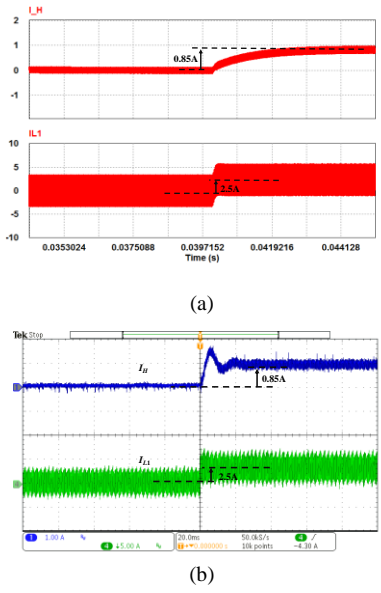
(a)



(b)

Fig. 22. Waveforms of controlled current step change in the low-voltage dual-source-powering mode: (a) by simulation; and (b) by measurement. ($i_H$ is changed from 0 to 0.85 A; $i_{L1}$ is changed from 0 to 2.5 A; Time/Div=20 ms/Div)
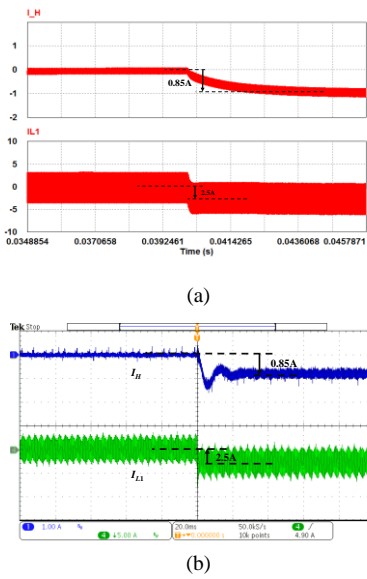


(a)



(b)

Fig. 23. Waveforms of controlled current step change in the high-voltage dc-bus energy-regenerating mode: (a) by simulation; and (b) by measurement. ($i_H$ is changed from 0 to -0.85 A; $i_{L1}$ is changed from 0 to -2.5 A; Time/Div=20 ms/Div)



(a)



(b)

Fig. 24. Waveforms of controlled current step change in the low-voltage dual-source boost mode: (a) by simulation; and (b) by measurement. ($i_{ES1}$ is changed from 0 to -6 A; $i_{L2}$ is changed from 0 to 12 A; Time/Div=20 ms/Div)



(a)



(b)
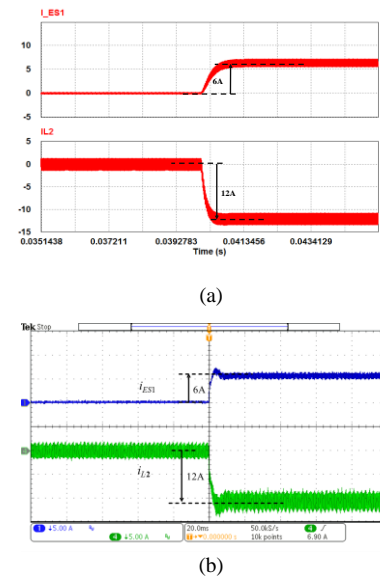
Fig. 25. Waveforms of controlled current step change in the low-voltage dual- source buck mode: (a) by simulation; and (b) by measurement. ($i_{ES1}$ is changed from 0 to 6 A; $i_{L2}$ is changed from 0 to 12 A; Time/Div=20 ms/Div)

that of those in Fig. 20(b), verifying the ability of the model to conduct bidirectional power flow between the main energy storage and the auxiliary energy storage. In summary, all the experimental results were very similar to the simulation results, and both sets of results were consistent with the predictions of the steady-state analyses.

Figs. 22 and 23 present the waveforms of a controlled current step change for the prototype system in the low-voltage dual-source-powering mode and in the high-voltage dc-bus energy-regenerating mode, respectively. As demonstrated in Fig. 22, the high-side current $i_H$ and the inductor current $i_{L1}$ were manipulated to deliver 360-W power from the low-side dual

sources to the high-side dc-bus. The negative current waveforms displayed in Fig. 23 indicate that the power flow was successfully reversed. Figs. 24 and 25 illustrate the waveforms of a controlled current step change for the prototype system in the low-voltage dual-source boost mode and in the low-voltage dual-source buck mode, respectively. As demonstrated in Fig. 24, the high-side current $i_{ES1}$ and the inductor current $i_{L2}$ were manipulated to deliver 576 W power between low-voltage dual-source. The negative current waveforms displayed in Fig. 25 indicate that the power flow was successfully reversed.
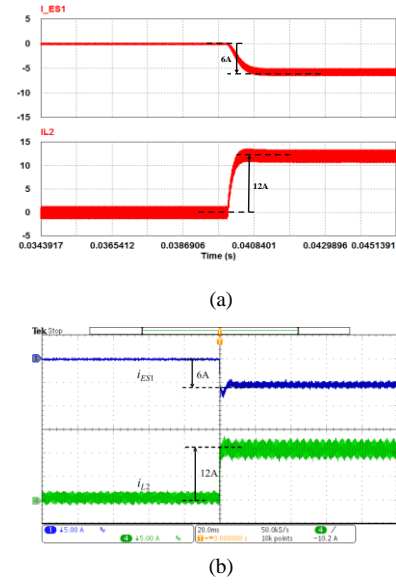
The current of main energy storage $i_{ES1}$ and the inductor current $i_{L2}$ were manipulated to deliver 580 W of power from the

Table III.
PERFORMANCE COMPARISON AMONG A VARIETY OF CONVERTERS.

| Items | Topology | | | | |
|---|---|---|---|---|---|
| | [25] | [34] | [35] | [36] | Proposed |
| Switching control structure | single-phase | single-phase | single-phase | four-phase | two-phase |
| Bidirectional power flow | Yes | No | No | Yes | Yes |
| Output ripple | Medium | High | Low | Low | Low |
| Number of PWM controlled switches | 6 | 5 | 4 | 8 | 6 |
| Passive components | 5 | 7 | 15 | 4 | 6 |
| Realized prototype power rating | 5 kW | 1 kW | 90 W | 5 kW | 1 kW |
| Maximum conversion efficiency | 91.5% | 94% | 93% | 95% | 97.25% |
| High-side voltage | 300 V | 400 V | 540 V | 200 V | 430 V |
| Low-side voltages | $V_{ES1}$: 125 V $V_{ES2}$: 144 V | $V_{ES1}$:30~50 V $V_{ES2}$: 50~100 V | $V_{ES1}$: 240~300 V $V_{ES2}$: 240~300 V | $V_{ES1}$: 42~63 V $V_{ES2}$: 48 V | $V_{ES1}$: 96 V $V_{ES2}$: 48 V |

the auxiliary energy storage to the main energy storage (Fig. 24). The negative current waveforms shown in Fig. 25 further confirm that power flow was successfully reversed. In summary, the experimental results presented in Figs. 22-25 closely patterned the simulation results. The efficiency of the proposed BDC under different load conditions was examined and the results are presented in Fig. 26. Its efficiency under 50-W to 1 kW experimental loads was above 88% for all modes of operation. Its conversion efficiency was measured using a precise digital power meter (Yokogawa-WT310).

As shown in Fig. 26, the highest conversion efficiencies of the high-voltage dc-bus energy-regenerative buck mode, low-voltage dual-source-powering mode, low-voltage dual-source boost mode (ES2 to ES1), and low-voltage dual-source buck mode (ES1 to ES2) were 97.25%, 95.32%, 95.76%, and 92.67%, respectively.

Performance comparisons of the proposed BDC and models presented in related studies are summarized in Table III. The models in [34] and [35] possessed a higher number of passive components than the proposed converter does. Moreover, the models therein do not possess bidirectional power flow capabilities. Although the converters in [25] and [36] featured bidirectional power flow, their corresponding maximum conversion efficiencies were lower than that of the converter proposed in this study. Additionally, the voltage conversion ratio of the proposed BDC is higher than that of the models presented in [25] and [34-36].
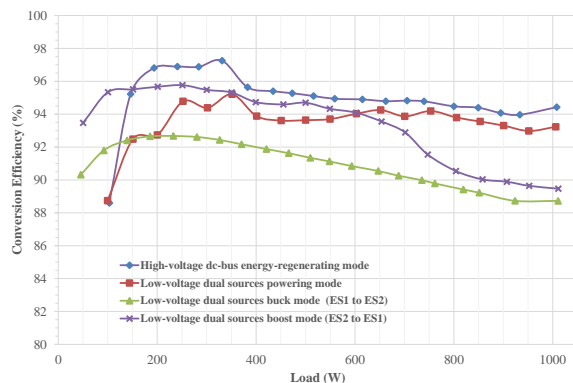


Fig. 26. Efficiency of the proposed BDC in different modes of operation under different load conditions.

For convenience, numerous active-power MOSFETs were adopted in the proposed BDC. However, only six power MOSFETs were switched using PWM-controlled signals. The power MOSFETs ($S_{ES1}$ and $S_{ES2}$) can be replaced with suitable breakers. Moreover, several commercial ES1 or ES2 packs include an on–off control function for shutting down the energy storage device; hence, the MOSFETs for $S_{ES1}$ and $S_{ES2}$ can be removed in future studies. In summary, compared with the works announced in [25] and [34-36], the proposed BDC topology achieved higher conversion efficiency, and bidirectional power flow, as well as lower output current and voltage ripples under 1 kW power loads. Furthermore, the price–performance ratio of the proposed BDC is higher than that of the aforementioned announced works.

## VI. POWER LOSS ANALYSIS

For further consideration for increasing the power rating of the proposed converter, the resulting loss breakdown charts are depicted in Figs. 27 and 29 as reference. Through estimated loss analysis of all components on four modes, it can be more understand that the influence of each component loss to converted efficiencies at different modes. Moreover, both situation of rising temperature and limitation of voltage or current stress are the major factor to damage components. Additionally, power loss estimation could be as reference before deciding specification of components, helping us to enhance the efficiencies of BDC. For simplicity the power loss estimation of switches include switching, conductive and driving loss, and the rest of all components such as capacitors and inductors only take conductive loss as a consideration.

The losing estimation of switches include switching, conductive and driving loss, and the rest of all components such as capacitors and inductors only take conductive loss as a consideration.

### A. Loss Analysis for Low-Voltage Dual-Source-Powering and High-Voltage DC-Bus Energy-Regenerating Modes

As shown in Fig. 27(a) and Fig. 27(b), the majority of loss is focus on inductors. The reason is both $I_{L1(rms)}$ and $I_{L2(rms)}$ are larger lead to substantial conductive loss. The only way to reduce conductive loss of inductors is to choose relatively lower equivalent of ESR. In addition, the loss and highest temperature of $Q_4$ is more than other switches because the conducted time is the longest and the $I_{Q4(rms)}$ is the biggest. By
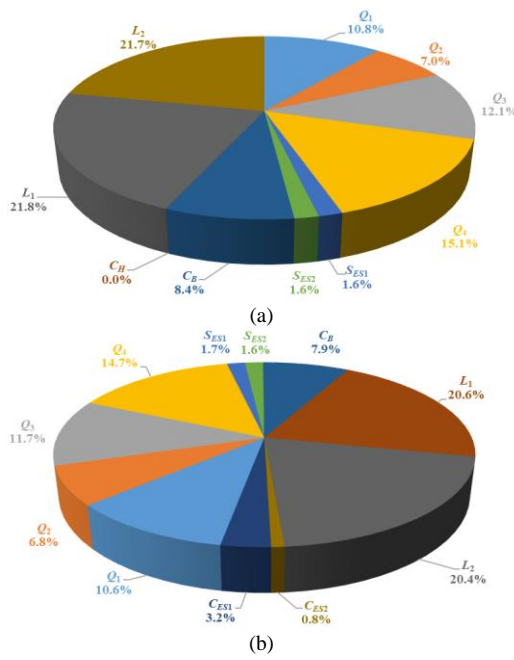
Fig. 27. Loss breakdown charts for (a) low-voltage dual-source-powering mode; and (b) high-voltage DC-Bus energy-regenerating modes.
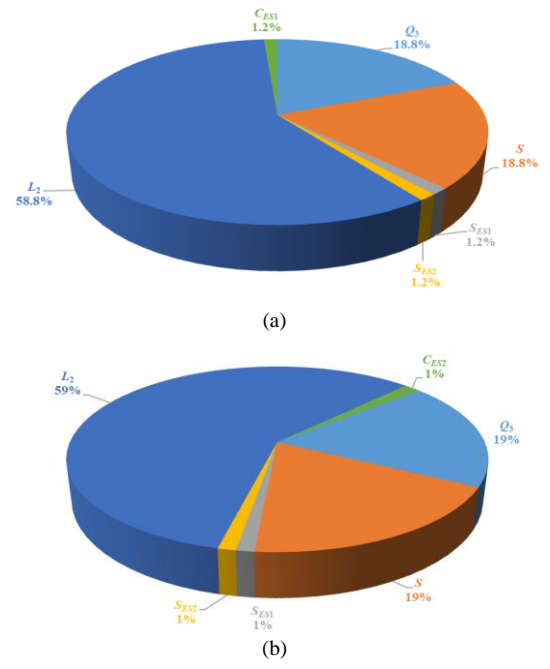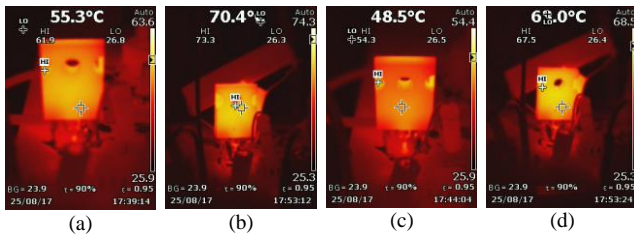


Fig. 28. Thermal image for low-voltage dual-source-powering mode: (a) $Q_2$ (b) $Q_4$; for high-voltage DC-Bus energy-regenerating mode: (c) $Q_2$ (d) $Q_4$.
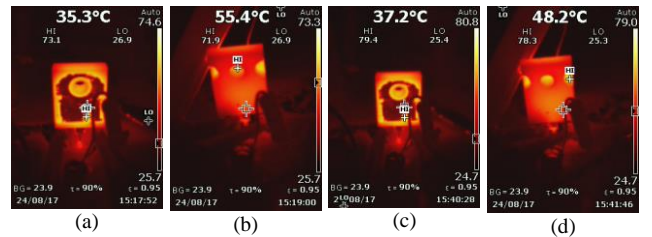


Fig. 29. Loss breakdown charts for (a) low-voltage dual-source boost mode; and (b) low-voltage dual-source boost mode.



Fig 30. Thermal image for low-voltage dual-source boost mode: (a) $Q_3$ (b) $S$; for low-voltage dual-source buck mode: (a) $Q_3$ (b) $S$.

contrast, the loss and highest temperature of $Q_2$ is the smallest because conducted time is the shortest and the $I_{Q2(rms)}$ is the smallest. As shown in Fig. 28, when proposed converter is operated at low-voltage dual-source-powering mode, the loss and temperature of both $Q_4$ and $Q_2$ would be significantly higher than high-voltage DC-Bus energy-regenerating mode. The results in the measured efficiency of low-voltage dual-source-powering mode are lower than that of high-voltage DC-Bus energy-regenerating mode.

### B. Loss Analysis for Low-Voltage Dual-Source Buck/Boost Mode

As shown in Fig. 29(a) and Fig. 29(b), the majority of loss is consumed on inductors. The reason is $I_{L2(rms)}$ is biggest lead to substantial conductive loss. The only way to reduce conductive loss of inductors is to choose relatively lower equivalent of ESR. In addition, the loss of $Q_3$ and $S$ are equivalent and their highest temperature are closed because $I_{Q3(rms)}$ and $I_{S(rms)}$ are quietly closed and their duty are basically the same. As shown in Fig. 30, when proposed converter is operated at low-voltage dual-source buck mode, the loss and temperature of both $Q_3$ and $S$ would be significantly higher than low-voltage dual-source boost mode.

The results in the measured efficiency of low-voltage dual-source buck mode are lower than that of low-voltage dual-source boost mode. It should be noticed that all images Fig. 28 and Fig. 30 was measured using an industrial thermal camera (Fluke-TiS75). It has automatic focus function to catch the highest temperature point of the device for the reliable results.

## VII. CONCLUSIONS

A new BDC topology was presented to interface dual battery energy sources and high-voltage dc bus of different voltage levels. The circuit configuration, operation principles, analyses, and static voltage gains of the proposed BDC were discussed on the basis of different modes of power transfer. Simulation and experimental waveforms for a 1 kW prototype system highlighted the performance and feasibility of this proposed BDC topology. The highest conversion efficiencies were 97.25%, 95.32%, 95.76%, and 92.67% for the high-voltage dc-bus energy-regenerative buck mode, low-voltage dual-source-powering mode, low-voltage dual-source boost mode (ES2 to ES1), and low-voltage dual-source buck mode (ES1 to ES2), respectively. The results demonstrate that the proposed BDC can be successfully applied in FC/HEV systems to produce hybrid power architecture (has been patented [37]).

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